Viking Technology

DFC4

Datasheet

Viking Discrete Flash Card (DFC) modules are case-less connector-less Discrete Flash Card cards which have a BGA footprint for direct soldering to PCBs. These rugged board-mounted SSD's are designed for harsh environments and eliminate the potential reliability issues associated with removable Discrete Flash Card cards. Ideal for storing OS software or microcode, Viking DFC's are ideal for embedded real time processing or for mobile low power applications.

REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	March 12, 2013	Initial release planer design (1445 PCB) using F3 controller	Sankar Shanmugam
A1	May 6, 2013	Add Cisco PN decoder	
A2	June 26, 2013	Revise PN table for rev C firmware	

Legal Information

Viking High Performance DFC Ordering Information

Part Number	Raw Capacity	Unformatted Capacity (bytes)	SLC NAND Device
VRFDFC40128EC6C-P1	128MB	127,401,984	128MB SLC, 1Gb BGA NAND Spansion S34ML01G100BHI000, RoHS
VIFDFC40128EC6C-P1	128MB	127,401,984	128MB SLC, 1Gb BGA NAND Spansion S34ML01G100BHI000,Leaded
VRFDFC40256EC9C-P1	256MB	254,803,968	256MB SLC, 2Gb BGA NAND Spansion S34ML02G100BHI000, RoHS
VIFDFC40256EC9C-P1	256MB	254,803,968	256MB SLC, 2Gb BGA NAND Spansion S34ML02G100BHI000, Leaded
VRFDFC40512EC7C-P1	512MB	531,062,784	512MB SLC, 4Gb BGA NAND Spansion S34ML04G100BHI000, RoHS
VRFDFC41024ECEC-MD	1GB	1,046,126,592	1GB SLC, 8Gb BGA NAND Micron MT29F8G08ADADAH4:D, RoHS
VIFDFC41024ECEC-MD	1GB	1,046,126,592	1GB SLC, 8Gb BGA NAND Micron MT29F8G08ADADAH4:D, Leaded

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1 Introduction

The Viking Discrete Flash Card (DFC) card is a single-channel, high-performance solution for a wide array of storage applications. Available in capacity ranges from 128MB to 2GB with a standard Viking Discrete Flash Card interface, system designers have an easy way to add small-form factor, reliable storage to any system at a fraction of the size of a hard disk drive.

Viking's rugged industrial designed SSD's offer the highest flash storage reliability and performance in harsh environments such as shock, vibration, humidity, altitude, ESD, and extreme temperatures.

Viking can also provide specialized services to OEMs designing customized hardware and systems by offering:

- Locked BOM control with customer product change notification (PCN)
- Pre-installed software, custom software imaging and ID strings
- Custom packaging and labeling
- Customer specified testing
- Conformal coating
- Localized Field Application Engineering for complete pre and post sale technical support

1.1 Features

The main features of Viking Discrete Flash Card memory controller are:

- Full support for SLC NAND flash memories
- Built-in ATA / PC card Interface
- Host data transfer rate in PIO mode 6 or MDMA mode 4 up to 25 MB/s
- Host data transfer rate in UDMA mode 4 up to 66 MByte/s
- Supports True-IDE mode
- Patented power fail management
- Embedded Reed-Solomon ECC, 4 symbols in a 512B sector
- Advanced global wear leveling
- Automatic power-down mode and sleep mode
- Industrial and commercial temperature
- ESD protection

1.2 Performance

Table 1-1: DFC Read/Write Performance

Parameter	Size	Value
Sequential Read	256K	up to 45 MB/s
Sequential Write	256K	up to 30 MB/s
Random Read	4K	up to 3098 IOPS
Random Write	4K	up to 23 IOPS

Note: 1) Measured using IOMETER 2006.
2) Performance may vary under extreme temperatures.

1.3 CHS Parameters

Table 1-2: CHS Parameters

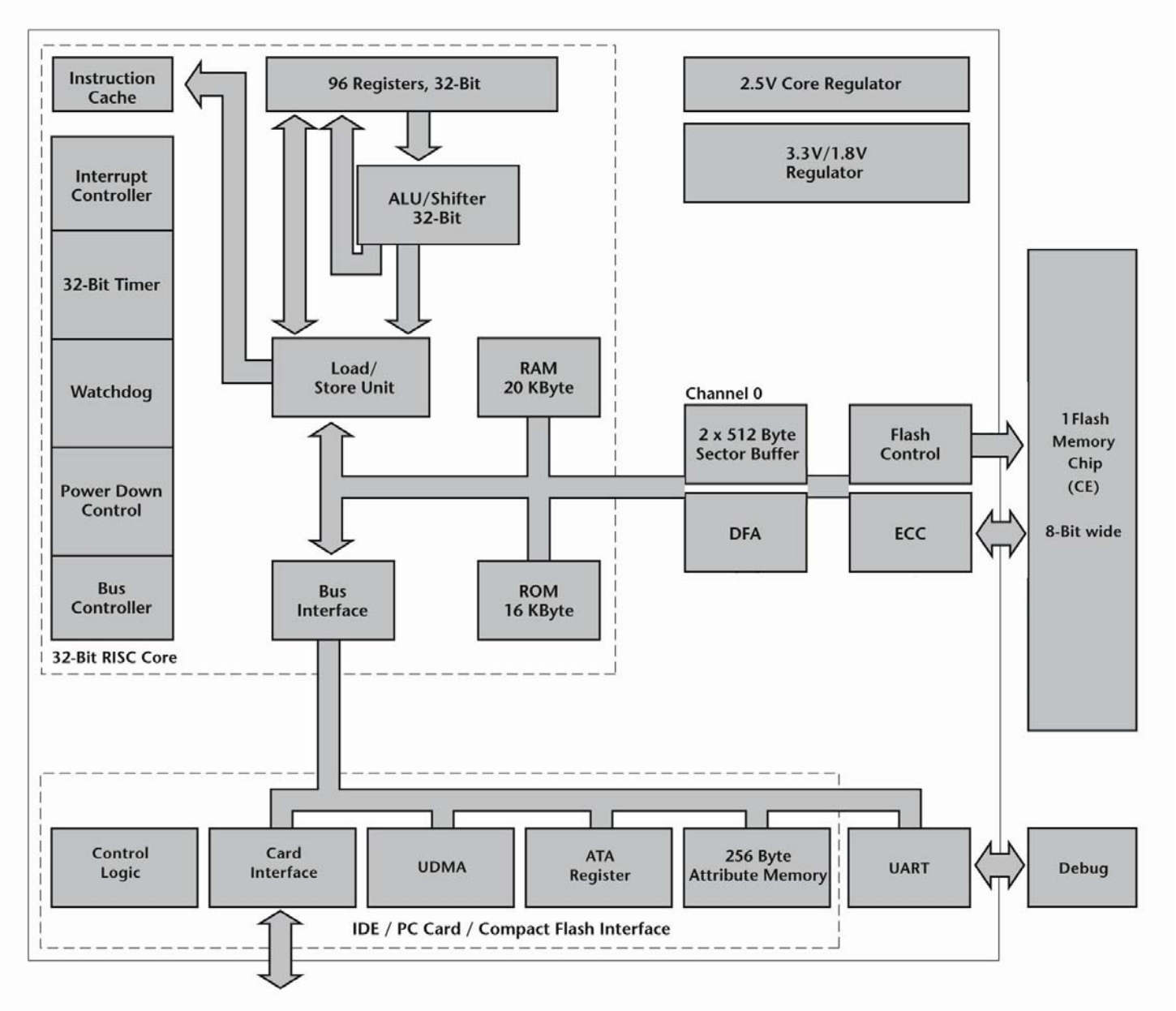
Capacity	Logical Block Addresses (LBA)	Cylinders (C) (standard)	Heads (H)	Sectors/Track (S)
128MB	248,832	486	16	63
256MB	497,664	972	16	63
512MB	1,037,232	1,029	16	63
1GB	2,043,216	2,027	16	63
2GB	3,992,688	3,961	16	63

Note: The unformatted capacity of the card may be less than the perceived or stated capacity on the label. Please use the LBA count in this table for reference.

*16,383 is the max Cylinder size for True IDE mode. Use total LBA to calculate size when using True IDE mode.

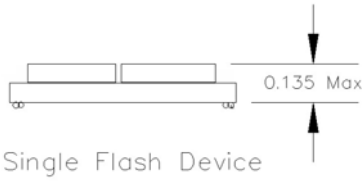
1.4 Block Diagram

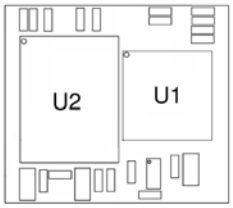
Figure 1-1: Functional Block Diagram



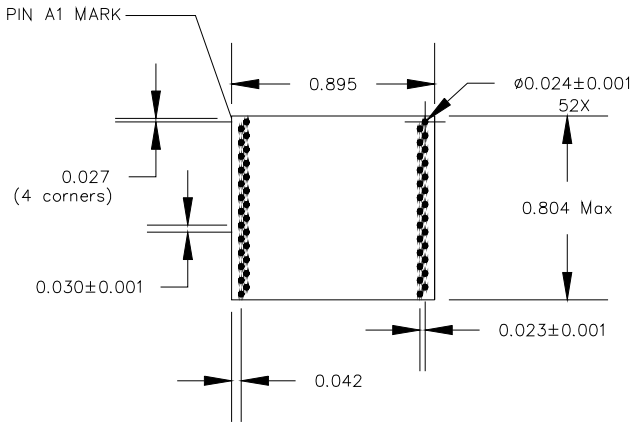
1.5 Mechanical Information

Figure 1-2: Dimensions





Top View showing components

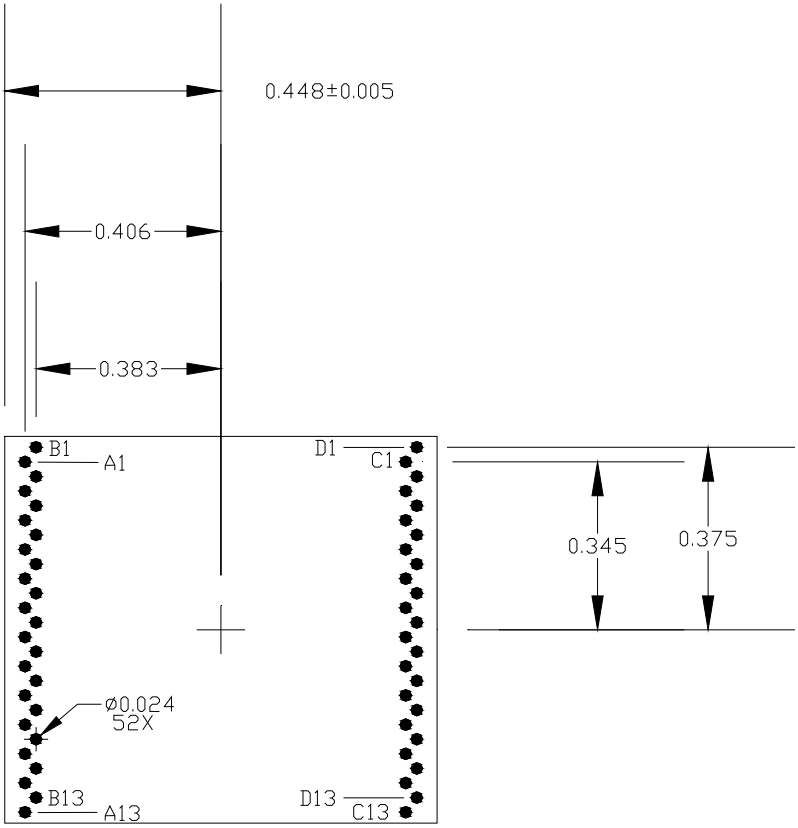


Top View
(Through device)

Note: 1) All dimensions are in inches. (Tolerance is +/- 0.005, unless otherwise stated.)
2) Height: 0.135" max

1.6 RECOMMENDED PCB FOOTPRINT AND PAD NUMBERS

All dimensions are in inches. (Tolerance is +/- 0.001, unless otherwise stated.)



Note: The pattern is the footprint/placement for the PCB (shown looking down through the DFC)

1.7 Interface

1.7.1 Host Interface

- Compatible with PCMCIA 2.1, PC Card ATA,
- Compatible with CF 3.0, CF 4.1 software command set
- ATA-6 standard compatible in True-IDE mode
- Memory mapped or I/O operation
- Fast ATA host-to-buffer transfer rates supporting PIO mode 6, MDMA mode 4, UDMA mode 4 in True-IDE mode
- Automatic sensing of PCMCIA or True-IDE host interface mode
- 4 integrated 8 Kbyte Sector Buffers & 256 Byte PCMCIA Attribute Memory
- PCMCIA Configuration Option Register, Card Configuration and Status Register and Pin Replacement Register support

2 Connector Pins

2.1 Connector Pin Assignments

Table 2-1: Connector Pin Assignments

Pin	Signal Name Memory / I/O / IDE	Pin	Signal Name Memory / I/O / IDE	Pin	Signal Name Memory / I/O / IDE	Pin	Signal Name Memory / I/O / IDE
A1	D8 / D8 / D8	B1	D1 / D1 / D1	C1	VSS/ VSS/ VSS	D1	VCC / VCC / VCC
A2	BVD1 / #STSCHG / #PDIAG	B2	D0 / D0 / D0	C2	VSS/ VSS/ VSS	D2	VCC / VCC / VCC
A3	BVD2 / #SPKR / #DASP	B3	A0 / A0 / A0	C3	VSS/ VSS/ VSS	D3	D2 / D2 / D2
A4	#REG / #REG / #DMACK	B4	A1 / A1 / A1	C4	D9 / D9 / D9	D4	WP / #IOIS16 / #IOCS16
A5	#INPACK / #INPACK / DMARQ	B5	A2 / A2 / A2	C5	D10 / D10 / D10	D5	A4 / A4 / A4
A6	#WAIT / #WAIT / IORDY	B6	A3 / A3 / A3	C6	A5 / A5 / A5	D6	#CSEL / #CSEL / #CSEL
A7	RESET / RESET / #RESET	B7	#CE2 / #CE2 / #CS1	C7	A6 / A6 / A6	D7	RDY / #IREQ / INTRQ
A8	#CE1 / #CE1 / #CS0	B8	D15 / D15 / D15	C8	A7 / A7 / A7	D8	#WE / #WE / #WE
A9	D7 / D7 / D7	B9	D14 / D14 / D14	C9	A8 / A8 / A8	D9	#IOWR / #IOWR / #IOWR
A10	D6 / D6 / D6	B10	D13 / D13 / D13	C10	A9 / A9 / A9	D10	#IORD / #IORD / #IORD
A11	D5 / D5 / D5	B11	D12 / D12 / D12	C11	#OE / #OE / #ATA SEL	D11	A10 / A10 / A10
A12	VSS / VSS / VSS	B12	VSS / VSS / VSS	C12	D3 / D3 / D3	D12	D11 / D11 / D11
A13	VCC / VCC / VCC	B13	VCC / VCC / VCC	C13	D4 / D4 / D4	D13	VSS/ VSS/ VSS

2.2 Pin Function Description

Table 2-2: Pin Function Description

Signal	(Mode) Function	Type	Description
A0 ~ A10	(All) Address	Input	In I/O and Memory modes, these are the Host Address lines that select the I/O port address registers or the memory mapped port address registers, and the control and status registers. In True IDE mode, only A0 ~ A2 are used to select the control, status and data register; A3 ~ A10 are not used.
#ATA SEL	(IDE) ATA Select	Input	Grounded to enable True IDE Mode.
BVD1 ~ BVD2	(Memory) Battery Voltage Detect	Output	Always asserted high since a battery is not used in this card.
#CE1 ~ #CE2	(I/O, Memory) Card Enable	Input	Select the card and indicates to the controller whether a byte or word operation is being performed. #CE2 always accesses the odd byte of the word; #CE1 accesses the even or odd byte of the word depending on the status of A0 and #CE2.
#CS0 ~ #CS1	(IDE) Chip Select	Input	#CS0 selects the ATA Command Block Registers; #CS1 selects the ATA Control Block Registers.
#CSEL	(All) Cable Select	Input	Signal is not used for I/O or memory mode, but should be grounded by the host. In IDE mode, configures the drive as a Master or Slave. If driven low, the drive is configured as a Master. If the pin is open, the drive is configured as a slave.
D0 ~ D15	(All) Host Data Bits	Input/ Output	These bi-directional signals carry the data, commands, and status information between the host and the controller.
#DASP	(IDE) Active/Slave Present	Input	Device active / Slave Present signal.
#DMACK	(IDE) DMA Acknowledge	Input	Signal that is asserted by the host in response to DMARQ to initiate DMA transfers.
DMARQ	(IDE) DMA Request	Output	This signal is used for DMA data transfers. The module asserts this signal when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by #IORD and #IOWR. This signal is used in a handshake manner with #DMACK. The device waits until the host asserts #DMACK before negating DMARQ, and reasserts DMARQ if there is more data to transfer.
#IREQ	(Memory, I/O) Interrupt Request	Output	Strobed low to generate a pulse mode interrupt. Held low for a level mode interrupt.
INTRQ	(IDE) Interrupt Request	Output	Interrupt Request to the Host (active high).
#INPACK	(I/O) Input Acknowledge	Output	Asserted when the card is selected and can respond to an I/O cycle at the address on the bus. The host uses this signal to control the enable of any input data buffers between the card and host system data bus.
IORDY	(IDE) I/O Channel Ready	Output	In True IDE mode, this is the active high I/O Channel Ready signal, where a low signal indicates that the controller is NOT ready and the host should extend the cycle for the present command.
#IOCS16	(IDE) 16 bit I/O	Output	Indicates a 16-bit transfer is in progress on the host bus. Open collector output.

Signal	(Mode) Function	Type	Description
#IOIS16	(I/O) 16 bit I/O	Output	Selects the 16-bit port. A low signal indicates that a 16-bit port is being addressed or an odd-byte-only operation can be performed at the addressed port.
#IORD	(All) I/O Read	Input	Clocks I/O data from the internal controller to the card bus.
#IOWR	(All) I/O Write	Input	Clocks I/O data from the card bus to the internal controller.
#OE	(I/O, Memory) Output Enable	Input	This input signal is used to enable Memory Read data from the memory card. In Memory mode it is used to read data and the CIS and Configuration registers. In I/O mode, this signal is used to read the CIS and Configuration registers only.
N/C	(All) No Connect	-	Not connected or used on the module.
#PDIAG	(IDE) Passed Diagnostics	Output	Used between two drives to indicate that the drive in Slave mode has passed diagnostics.
RDY	(Memory) Ready	Output	This signal is set high when the card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the card has completed its power up or reset function. No access of any type should be made to the card during this time.
#REG	(I/O, Memory) Register Memory Select	Input	In Memory mode, this input signal distinguishes the register (attribute) memory from the common memory. In I/O mode, this signal must be asserted (low) when the I/O address is on the bus.
RESET	(I/O, Memory) Reset	Input	The controller is reset when this signal is asserted (high), initializing the control and status registers and aborting any command in progress.
#RESET	(IDE) Reset	Input	The controller is reset when this signal is asserted (low), initializing the control and status registers and aborting any command in progress.
#SPKR	(I/O) Speaker	Output	Always low; speaker not supported by the card.
#STSCHG	(I/O) Status Changed	Input / Output	Indicates a change in RDY/#BSY or Write Protect states.
#WAIT	(I/O, Memory) Input/Output Data Ready	Output	In Memory and I/O modes, this output is driven by the controller to signal the host to insert a delay before completing a memory or I/O cycle.
#WE	(I/O, Memory) Write Enable	Input	In Memory mode, strobes Memory Write data into the card. In both Memory mode and I/O mode, this signal is used for writing the configuration register, in conjunction with the #REG signal. Not used in IDE mode, connect to VCC.
WP	(Memory) Write Protect	Output	Driven low after the completion of the reset initialization sequence.
VCC	Voltage Supply	Power	These pins supply 3.3V to the DFC.
VSS	Ground	Gnd	These pins supply ground to the DFC.

Notes: 1. PU= internal pullup, PD= internal pull down.

3 Product Specifications

3.1 Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	-0.3 ~ 4.6	V
Input Voltage	VIN	GND - 0.5 ~ VCC + 0.5	V
Output Voltage	VOUT	GND - 0.5 ~ VCC + 0.5	V
Storage Temperature	TST	-65° to + 150°	°C

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

3.2 DC Operating Conditions and Characteristics

Recommended operating conditions (Voltages referenced to GND, TA = 0 to 70°C)

Table 3-2: DC Operating Conditions and Characteristics

Symbol	Parameter	Min	Max	Units	Notes
VIL	Input LOW Voltage	-0.3	+0.8	V	
VIH	Input HIGH Voltage	2.0	VCC+0.3	V	
VOL	Output LOW Voltage		0.45	V	at 4mA (12mA for DASP)
VOH	Output HIGH Voltage	2.4		V	at 1mA
ICC	Operating Current Sleep mode Operating, 20 MHz Operating, 40 MHz		0.35 45 80	mA mA mA	typical 0.2mA typical 30mA typical 50mA
ILI	Input Leakage Current		±10	µA	if not pull-up/pull-down
ILO	Output Leakage Current		±10	µA	

3.3 Environmental Specifications

Table 3-3: Environmental Specifications

Parameter	Value
Operating Temperature (Commercial Temp):	0 to 70c
Operating Temperature (Industrial Temp):	-40 to 85c
Humidity (non-condensing):	5% to 95% non-condensing

3.4 Reliability & Retention

Table 3-4: DFC Reliability and Retention

Parameter	Value
Data Reliability	Bit Error rate 10E-15
Data Retention	10 Years

3.5 Capacitance

Table 3-5: Capacitance

Parameter	Symbol	Min.	Max.	Unit
Input capacitance	Cin	-	10	pF
Output capacitance	Cout	-	10	pF

3.6 AC Characteristics

Input rise and fall time requirements: Input rise and fall time should be 10ns or less.

3.6.1 Power-on Timing

Table 3-6: Power-on Timing

Parameter	Symbol	Min	Typ	Max	Unit
Card Enable setup time	tsu(VCC)	275.01	-	-	ms
VCC detect to RST disable	tRPU	100	150	250	ms
Host RESET Hi-z hold time	th(Hi-z RESET)	255	-	-	ms
Host RESET width	tw(RESET)	10us	-	20ms	-
Host RESET setup time	tsu(RESET)	20	-	-	ms

Note: See Figure 1 for details.

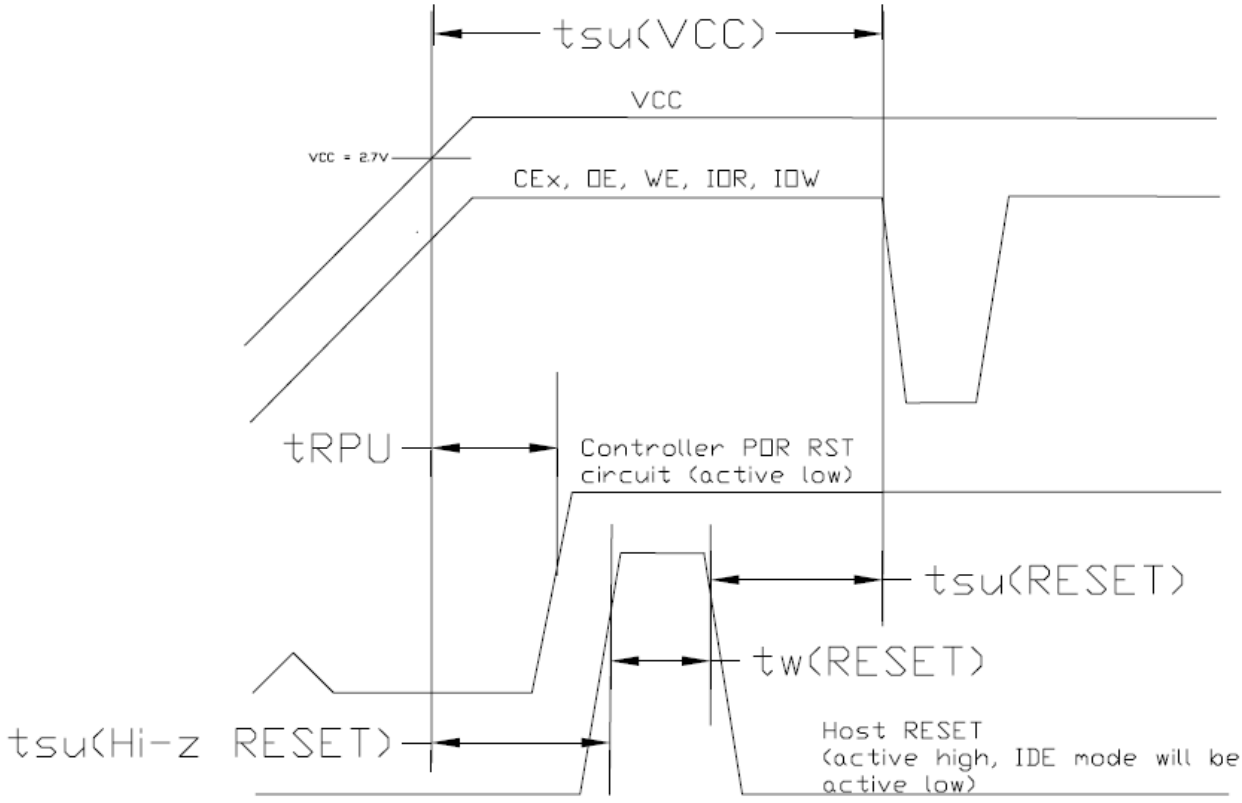


Figure 3-1: Power On RESET Timing

3.6.2 Attribute Memory Read / Write Timing

Table 3-7: Attribute Memory Read Write Timing

Symbol	Parameter	Min	Max	Units
tcR	Read cycle time	250		ns
ta(A)	Address access time		250	ns
ta(CE)	Card Enable access time		250	ns
ta(OE)	Output Enable access time		125	ns
tdis(CE)	Output disable time from CE		100	ns
tdis(OE)	Output disable time from OE		100	ns
ten(CE)	Output enable time from CE	5		ns
ten(OE)	Output enable time from OE	5		ns
tv(A)	Data valid time from address change	0		ns
tsu(A)	Address setup time	30		ns
th(A)	Address hold time	20		ns
tsu(CE)	Card Enable setup time	0		ns
th(CE)	Card Enable hold time	20		ns
tcW	Write cycle time	250		ns
tw(WE)	Write pulse time	150		ns
tsu(A)	Address setup time for WE	30		ns
tsu(CE)	Card Enable setup time for WE	30		ns
tsu(D-WEH)	Data setup time for WE	80		ns
th(D)	Data hold time	30		ns
tdis(WE)	Output disable time from WE		100	ns
ten(WE)	Output enable time from WE	5		ns
tsu(OE-WE)	Output Enable setup time for WE	10		ns
th(OE-WE)	Output Enable hold time from WE	10		ns

3.6.3 Common Memory Read and Write Characteristics

Table 3-8: Common Memory Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
tcR	Read cycle time	80		ns
ta(A)	Address access time		55	ns
ta(CE)	Card Enable access time		55	ns
ta(OE)	Output Enable access time		45	ns
tdis(CE)	Output disable time from CE		45	ns
tdis(OE)	Output disable time from OE		45	ns
ten(CE)	Output enable time from CE	5		ns
ten(OE)	Output enable time from OE	5		ns
tv(A)	Data valid time from address change	0		ns
tsu(A)	Address setup time	10		ns
th(A)	Address hold time	10		ns
tsu(CE)	Card Enable setup time	0		ns
th(CE)	Card Enable hold time	10		ns
tcW	Write cycle time	80		ns
tw(WE)	Write pulse time	55		ns
tsu(A)	Address setup time for WE	10		ns
tsu(CE)	Card Enable setup time for WE	0		ns
tsu(D-WEH)	Data setup time for WE	30		ns
th(D)	Data hold time	10		ns
trec(WE)	Write recover time	15		ns
tdis(WE)	Output disable time from WE		45	ns
ten(WE)	Output enable time from WE	5		ns
tsu(OE-WE)	Output Enable setup time for WE	10		ns
th(OE-WE)	Output Enable hold time from WE	10		ns

3.6.4 I/O Access Read and Write Characteristics

Table 3-9: I/O Access Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
td(IORD)	Data delay after IORD		45	ns
th(IORD)	Data hold following IORD	5		ns
tw(IORD)	IORD pulse width	55		ns
tsuA(IORD)	Address setup time for IORD	15		ns
thA(IORD)	Address hold time from IORD	10		ns
tsuCE(IORD)	Card Enable setup time for IORD	5		ns
thCE(IORD)	Card Enable hold time from IORD	10		ns
tsuREG(IORD)	REG setup time for IORD	5		ns
thREG(IORD)	REG hold time from IORD	0		ns
tdfINP(IORD)	INPACK delay falling from IORD	0	45	ns
tdrINP(IORD)	INPACK delay rising from IORD		45	ns
tdfIO16(IORD)	IOIS16 delay falling from address		35	ns
tdrIO16(IORD)	IOIS16 delay rising from address		35	ns
tsu(IOWR)	Data setup time for IOWR	15		ns
th(IOWR)	Data hold time from IOWR	5		ns
tw(IOWR)	IOWR pulse width	55		ns
tsuA(IOWR)	Address setup time for IOWR	15		ns
thA(IOWR)	Address hold time from IOWR	10		ns
tsuCE(IOWR)	Card Enable setup time for IOWR	5		ns
thCE(IOWR)	Card Enable hold time from IOWR	10		ns
tsuREG(IOWR)	REG setup time for IOWR	5		ns
thREG(IOWR)	REG hold time from IOWR	0		ns

3.6.5 True-IDE PIO Mode Read and Write Characteristics

Table 3-10: True-IDE PIO Mode Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
t0	Cycle time	80		ns
t1	Address setup time for IORD/IOWR	10		ns
t9	Address hold time from IORD/IOWR	10		ns
t2	IORD/IOWR pulse width	55		ns
t2i	IORD/IOWR recovery time	20		ns
t5	Data setup time for IORD	10		ns
t6	Data hold following IORD	5		ns
t6z	Output disable time from IORD		20	ns
t3	Data setup time for IOWR	15		ns
t4	Data hold following IOWR	5		ns

3.6.6 True-IDE MDMA Mode Read and Write Characteristics

Table 3-11: True-IDE MDMA Mode Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
tO	Cycle time	80		ns
tD	IORD/IOWR pulse width	55		ns
tE	IORD data access		45	ns
tF	Data hold following IORD	5		ns
tG	Data setup time for IORD/IOWR	10		ns
tH	Data hold following IOWR	5		ns
tI	DMACK setup time for IORD/IOWR	0		ns
tJ	DMACK hold following IORD/IOWR	5		ns
tKR, tKW	IORD/IOWR recovery time	20		ns
tLR, tLW	IORD/IOWR to DMARQ delay		35	ns
tM	CS0, CS1 setup for IORD/IOWR	5		ns
tN	CS0, CS1 hold following IORD/IOWR	10		ns
tZ	Output disable time from DMACK		25	ns

3.6.7 CF-ATA Command Support

Table 3-12: CF-ATA Command Support

No.	Command	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check Power Mode	E5h, 98h	--	--	--	--	Y	--	--
2	Erase Sector	C0h	--	Y	Y	Y	Y	Y	Y
3	Execute Drive Diagnostic	90h	--	--	--	--	--	--	--
4	Flush Cache	E7h	--	--	--	--	Y	--	--
5	Format Track	50h	--	Y	--	Y	Y	Y	Y
6	Identify Drive	ECh	--	--	--	--	Y	--	--
7	Idle	E3h, 97h	--	Y	--	--	Y	--	--
8	Idle Immediate	E1h, 95h	--	--	--	--	Y	--	--
9	Initialize Drive Parameters	91h	--	Y	--	--	Y	Y	--
10	Media Lock	DEh	--	--	--	--	Y	--	--
11	Media Unlock	DFh	--	--	--	--	Y	--	--
12	NOP	00h	--	--	--	--	Y	--	--
13	Read Buffer	E4h	--	--	--	--	Y	--	--
14	Read DMA	C8h, C9h	--	Y	Y	Y	Y	Y	Y
15	Read Multiple	C4h	--	Y	Y	Y	Y	Y	Y
16	Read Long	22h, 23h	--	--	Y	Y	Y	Y	Y
17	Read Native Max Address	F8h	--	--	--	--	Y	--	--
18	Read Sector(s)	20h, 21h	--	Y	Y	Y	Y	Y	Y
19	Read Verify Sector(s)	40h, 41h	--	Y	Y	Y	Y	Y	Y
20	Recalibrate	1Xh	--	--	--	--	Y	--	--
21	Request Sense	03h	--	--	--	--	Y	--	--
22	Security Disable Password	F6h	--	--	--	--	Y	--	--
23	Security Erase Prepare	F3h	--	--	--	--	Y	--	--
24	Security Erase Unit	F4h	--	--	--	--	Y	--	--
25	Security Freeze Lock	F5h	--	--	--	--	Y	--	--
26	Security Set Password	F1h	--	--	--	--	Y	--	--
27	Security Unlock	F2h	--	--	--	--	Y	--	--
28	Seek	7Xh	Y	--	--	--	Y	--	--
29	Set Feature	EFh	--	Y	Y	Y	Y	Y	Y
30	Set Max Address	F9h	--	Y	Y	Y	Y	Y	Y
31	Set Multiple Mode	C6h	--	Y	--	--	Y	--	--
32	Set Sleep Mode	E6h, 99h	--	--	--	--	Y	--	--
33	SMART	B0h	Y	Y	--	Y	Y	--	--
34	Standby	E2h, 96h	--	Y	--	--	Y	--	--
35	Standby Immediate	E0h, 94h	--	--	--	--	Y	--	--
36	Translate Sector	87h	--	Y	Y	Y	Y	Y	Y
37	Write Buffer	E8h	--	--	--	--	Y	--	--
38	Write DMA	CAh, CBh	--	Y	Y	Y	Y	Y	Y
39	Write Long	32h, 33h	--	--	Y	Y	Y	Y	Y

No.	Command	Code	FR	SC	SN	CY	DR	HD	LBA
40	Write Multiple	C5h	--	Y	Y	Y	Y	Y	Y
41	Write Multiple w/o Erase	CDh	--	Y	Y	Y	Y	Y	Y
42	Write Sector(s)	30h, 31h	--	Y	Y	Y	Y	Y	Y
43	Write Sector(s) w/o Erase	38h	--	Y	Y	Y	Y	Y	Y
44	Write Verify	3Ch	--	Y	Y	Y	Y	Y	Y

Notes: Abbreviations in this table:

- FR: Features Register
- SC: Sector Count Register (00h – FFh; 00h means 256 sectors
- SN: Sector Number Register
- CY: Cylinder Low/ High Register
- DR: Drive bit of Drive/Head Register
- HD: Head Number (0-15) of Drive/ Head Register
- LBA: Logic Block Address Mode Support
- --: Not used for this command
- Y: Used for this command

3.7 Capacity Information

3.7.1 True IDE Mode

Table 3-13: True IDE Mode

Card Size	Cylinders (Note 1)	Head	Sector	Total Sectors (Note 2, 3)	Usable Capacity (bytes)
128MB	486	16	32	248,832	127,401,984
256MB	972	16	32	497,664	254,803,968
512MB	1029	16	63	1,037,232	531,062,784
1GB	2027	16	63	2,043,216	1,046,126,592
2GB	3961	16	63	3,992,688	2,044,256,256

Notes:

1. Total sectors remaining after deducting firmware and spare block overhead.
2. Available data capacity is dependent on format and partition type.

3.7.2 PCMCIA Mode (I/O and Memory Modes)

Table 3-14: PCMCIA Mode (I/O and Memory Modes)

Card Size	Cylinders (Note 1)	Head	Sector	Total Sectors (Note 2, 3)	Usable Capacity (bytes)
128MB	486	16	32	248,832	127,401,984
256MB	972	16	32	497,664	254,803,968
512MB	1029	16	63	1,037,232	531,062,784
1GB	2027	16	63	2,043,216	1,046,126,592
2GB	3961	16	63	3,992,688	2,044,256,256

Notes:

1. Total sectors remaining after deducting firmware and spare block overhead.
2. Available data capacity is dependent on format and partition type.

3.8 Identify Drive Parameter

An example of the parameter information received from the DFC when invoking the Identify Drive command (ECh) is listed in table below:

Table 3-15: Identify Drive Parameter

Word Address	Default Value	Bytes	Data Field Type Information
0	045AH	2	General configuration bit-significant information
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	0200H	2	Number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7 - 8	XXXXH	4	Number of sectors per DFC
9	0000H	2	Reserved
10 - 19	XXXXH	20	Serial Number in ASCII (20 characters)
20	0002H	2	Buffer type (dual-ported multi-sector)
21	0001H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long commands
23 - 26	XXXXH	8	Firmware revision (8 ASCII characters)
27 - 46	XXXXH	40	Model Number in ASCII (40 characters)
47	8001H	2	Maximum 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0F00H	2	Capabilities: DMA, LBA, IORDY supported
50	4001H	2	Capabilities: device specific standby timer minimum
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	DMA data transfer cycle timing mode not supported
53	0007H	2	Data Fields 54 – 58, 64 – 70, and 88 are valid
54	XXXXH	2	Number of Current Logical Cylinders
55	XXXXH	2	Number of Current Logical Heads
56	XXXXH	2	Number of Current Logical Sectors Per Track
57 - 58	XXXXH	4	Current Capacity in Sectors
59	010XH	2	Multiple sector setting is valid
60 - 61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single word DMA transfer not implemented
63	0X0XH	2	Multiword DMA transfer mode
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum multiword DMA cycle time, 0 if no MDMA
66	0078H	2	Recommended multiword DMA cycle time, 0 if no MDMA
67	0078H	2	Minimum PIO cycle time without flow control
68	0078H	2	Minimum PIO cycle time with flow control
69 - 79	0000H	22	Reserved

Word Address	Default Value	Bytes	Data Field Type Information
80	0020H	2	Major version number, ATA-5 support
81	0000H	2	Minor version number, not reported
82	740BH	2	Command set: NOP, READ BUFFER, WRITE BUFFER, host protected area, power management feature set, Security Mode feature set, SMART feature set
83	5004H	2	Command set: FLUSH CACHE, CFA feature set
84	4000H	2	Command set/feature supported extension
85	740XH	2	Command set enabled: NOP, READ BUFFER, WRITE BUFFER, host protected area, power management feature set, Security Mode feature set enabled/disabled, SMART feature set enabled/disabled
86	1004H	2	Command set enabled: FLUSH CACHE, CFA feature set
87	4000H	2	Command set/feature default
88	XXXXH	2	UDMA mode
89	0000H	2	Time for Security Erase Unit not specified
90	0000H	2	Time for Enhanced Security Erase Unit not specified
91	0000H	2	Reserved
92	XXXXH	2	Master Password Revision Code
93	XXXXH	2	Hardware Reset Result
94 – 127	0000H	72	Reserved
128	0XXXH	2	Security Status
129	XX00H	2	Write Protect Status. Bit 15 = permanent write protect, no more spare blocks available
130 – 133	XXXXH	8	Firmware date string
134	848AH	2	General Configuration word for PCMCIA mode
135	045AH	2	General Configuration word for True-IDE mode
136 – 141	XXXXH	12	Firmware file name
142 – 147	XXXXH	12	Preformat file name
148 – 153	XXXXH	12	Anchor program file name
154 – 159	0000H	12	Reserved
160	A064H	2	CFA Power Mode: no power level 1, max 100mA
161	0000H	2	Reserved
162	0000H	2	Key Management Schemes: CPRM not supported
163	XXXXH	2	CFA advanced modes: supported and enabled bits
164	001BH	2	CFA advanced modes: 80ns I/O and Memory supported
165 – 254	0000H	180	Reserved
255	XXA5H	2	Integrity Word

Table 3-16: Identify Drive Parameter Table in PCMCIA mode showing word differences

Word Address	Default Value	Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information
49	0E00H	2	Capabilities: LBA, IORDY supported
63	0000H	2	Multi Word DMA transfer mode not supported
65	0000H	2	Minimum Multi Word DMA cycle time
66	0000H	2	Recommended Multi Word DMA cycle time
93	0000H	2	Hardware Reset Result not supported
163 - 164	0000H	4	CFA advanced modes: not supported

Table 3-17: Identify Drive Parameter Table in PCMCIA mode showing word differences

Word Address	Default Value	Bytes	Data Field Type Information
83	5000H	2	Command set: FLUSH CACHE
86	1000H	2	Command set enabled: FLUSH CACHE
160-164	0000H	10	Reserved

3.9 SMART Support

The Viking Firmware supports the following SMART commands, determined by the Feature Register value.

Table 3-18: Supported SMART Commands determined by Feature Register value

Value	Command
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute Autosave
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
E0h	SMART Read Remap Data
E1h	SMART Read Wear Level Data

SMART commands with Feature Register values not mentioned in the above table are not supported, and will be aborted.

3.9.1 SMART Enable Operations

COMMAND CODE | B0h with a Feature Register value of D8h
PROTOCOL | Non-data.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | None required.
ERROR OUTPUTS | Aborted if the signature in the Cylinder registers is invalid.
DESCRIPTION | This command enables access to the SMART capabilities of the firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

3.9.2 SMART Disable Operations

COMMAND CODE | B0h with a Feature Register value of D9h
PROTOCOL | Non-data.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | None required.
ERROR OUTPUTS | Aborted if either the signature in the Cylinder registers is invalid, or if SMART is not enabled.

DESCRIPTION | This command disables access to the SMART capabilities of the firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

3.9.3 SMART Enable/Disable Attribute Autosave

COMMAND CODE | B0h with a Feature Register value of D2h
PROTOCOL | Non-data.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count	00h or F1h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | None required.
ERROR OUTPUTS | Aborted if either the signature in the Cylinder registers is invalid, or if SMART is not enabled.
DESCRIPTION | This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the firmware.

3.9.4 SMART Read Data

COMMAND CODE | B0h with a Feature Register value of D0h
PROTOCOL | PIO data in.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | None required.
ERROR OUTPUTS | Aborted if either the signature in the Cylinder registers is invalid, or if SMART is not enabled.
DESCRIPTION | This command returns one sector of SMART data. The data structure returned is:

Offset	Value	Description
0..1	0004h	SMART structure version
2..361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364..365	0000h	Total time to complete off-line data collection
366	00h	
367	00h	Off-line data collection capability (no off-line data collection)
368..369	0003h	SMART capabilities
370	00h	Error logging capability (no error logging)
371	00h	
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374..385	00h	Reserved
386..387	0002h	SMART Version
388..391		Firmware “Commit” counter
392..395		Firmware Wear Level Threshold
396		Global Wear Leveling active
397		Global Bad Block Management active
398..510	00h	
511		Data structure checksum

There are six attributes that are defined for the firmware. These return their data in the attribute section of the SMART data, using a 12 byte data field.

The field at offset 386 gives a version number for the contents of the SMART data structure. For the controller, only version 2 is defined.

The byte at offset 396 is 0 if the wear leveling has not yet started its global operation and 1 if the global wear leveling has started. This happens when the most used chip has reached the erase count threshold defined in the Erase Count Attribute.

The byte at offset 397 is 0 if the bad block management is still working chip local, and 1 if the global bad block management has started. This happens when one of the flash chips runs out of spare blocks, in this case spare blocks from different flash chips are used.

3.9.4.1 Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1..2	0003h	Flags – Pre-fail type, attribute value is updated during normal operation
3		Attribute value. The value returned here is the percentage of remaining spare blocks summed over all flash chips, i.e. (100 x current spare blocks / initial spare blocks)
4..5		Initial number of spare blocks of the flash chip with the lowest current number of spare blocks
6..7		Current number of spare blocks of the flash chip with the lowest current number of spare blocks
8..9		Sum of the initial number of spare blocks for all flash chips
10..11		Sum of the current number of spare blocks for all flash chips

3.9.4.2 Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been performed.

Offset	Value	Description
0	229	Attribute ID – Erase Count Usage (vendor specific)
1..2	000Xh	Flags – Pre-fail or Advisory type, attribute value is updated during normal operation
3		Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block

		erases compared to the target number of erase cycles per block.
4..11		Estimated total number of block erases

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

3.9.4.3 Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of ECC errors (correctable and uncorrectable)
8..11		~

3.9.4.4 Correctable ECC Errors Attribute

This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of ECC errors (correctable and uncorrectable)
8..11		~

3.9.4.5 Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	232	Attribute ID – Number of Reads

1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..11		Total number of flash read commands

3.9.4.6 UDMA CRC Errors Attribute

This attribute gives information about the total number of UDMA CRC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	199	Attribute ID – UDMA CRC error rate
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of UDMA CRC errors
8..11		

3.9.5 SMART Read Attribute Thresholds

COMMAND CODE | B0h with a Feature Register value of D1h
PROTOCOL | PIO data in.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	D1h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | None required.
ERROR OUTPUTS | Aborted if either the signature in the Cylinder registers is invalid, or if SMART is not enabled.
DESCRIPTION | This command returns one sector of SMART attribute thresholds. The data structure returned is:

Offset	Value	Description
0..1	0004h	SMART structure version
2..361	0002h	Attribute threshold entries 1 to 30 (12 bytes each)
362..379	00h	Reserved
380..510	00h	

511		Data structure checksum

3.9.5.1 Spare Block Count Attribute Threshold

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1		Factory Programmed Spare Block Count Threshold
2..11	00h	Reserved

3.9.5.2 Erase Count Attribute Threshold

Offset	Value	Description
0	229	Attribute ID – Erase Count Usage
1		Factory Programmed Erase Count Threshold
2..11	00h	Reserved

3.9.5.3 Total ECC Errors Attribute Threshold

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1	00h	No threshold for the Total ECC Errors Attribute
2..11	00h	Reserved

3.9.5.4 Correctable ECC Errors Attribute

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1	00h	No threshold for the Correctable ECC Errors Attribute
2..11	00h	Reserved

3.9.5.5 Total Number of Reads Attribute

Offset	Value	Description
0	232	Attribute ID – Number of Reads
1	00h	No threshold for the Total Number of Reads Attribute
2..11	00h	Reserved

3.9.5.6 UDMA CRC Errors Attribute

Offset	Value	Description
0	199	Attribute ID – UDMA CRC error rate

1	00h	No threshold for the UDMA CRC Errors Attribute
2..11	00h	Reserved

3.9.6 SMART Return Status

COMMAND CODE | B0h with a Feature Register value of DAh
PROTOCOL | Non-data.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	DAh							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | Returns a status indication as described below.
ERROR OUTPUTS | Aborted if either the signature in the Cylinder registers is invalid, or if SMART is not enabled.
DESCRIPTION | This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

3.9.7 SMART Read Remap Data

COMMAND CODE | B0h with a Feature Register value of E0h
PROTOCOL | PIO data in.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	E0h							
Sector Count	01h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | None required.
ERROR OUTPUTS | Aborted if either the signature in the Cylinder registers is invalid, if the Sector Count is not 1, or if SMART is not enabled.

DESCRIPTION | This command returns one sector of spare block information. The information is the initial number of blocks per flash chip available for bad block remap, and the current number of blocks per flash chip available for bad block remap. The layout of the returned sector is:

Offset	Description
0..31	Initial number of replacement blocks for chips 0..15, 2 bytes per entry
32..63	Current number of replacement blocks for chips 0..15, 2 bytes per entry
64..511	

3.9.8 SMART Read Wear Level Data

COMMAND CODE | B0h with a Feature Register value of E1h
PROTOCOL | PIO data in.
INPUTS |

Register	7	6	5	4	3	2	1	0
Features	E1h							
Sector Count	04h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS | None required.

ERROR OUTPUTS | Aborted if either the signature in the Cylinder registers is invalid, if the Sector Count is not 4, or if SMART is not enabled.

DESCRIPTION | This command will return four sectors of information regarding the status of the wear leveling. The information returned is the distribution of the blocks into the 1024 possible wear level classes. For each of the wear level classes, the number of blocks that have this class is returned in the data sectors.

The layout of the returned sectors is, with n the sector number from 0 to 3:

Offset	Description
0..1	Number of flash blocks that have wear level class 256*n+0
2..3	Number of flash blocks that have wear level class 256*n+1
…	…
508..509	Number of flash blocks that have wear level class 256*n+254
510..511	Number of flash blocks that have wear level class 256*n+255

i.e. the first sector returns the information for wear level classes 0 to 255, the second sector returns the information for wear level classes 256 to 511, and so on.

A block moves from one wear level class into the next when it reaches the number of erases that is specified as the factory programmed “Wear Level Threshold”. A common threshold number is 4095, this means that blocks in wear level class 0 have seen 0 to 4095 erases, blocks in wear level class 1 have seen 4096 to 8191 erases, and so on. Using this information, statements about the wear of the card, and of the estimated remaining life can be made. The useful range of wear level classes is 0 to 1022, class 1023 has blocks that are not subject to wear leveling, like the Anchor block.

4 Certifications and Compliance

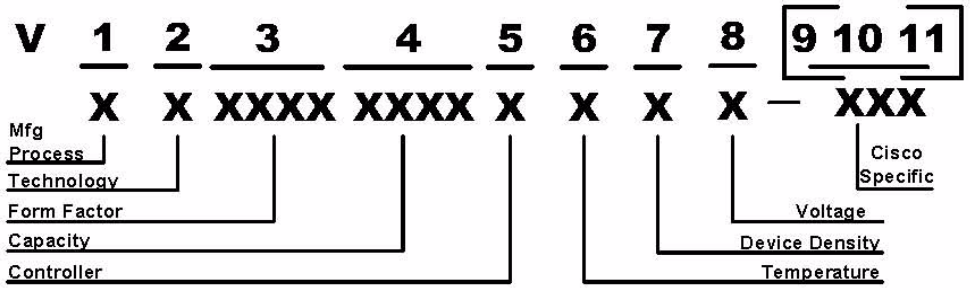
Table 4-1: Device Certifications

Certification/Compliance	Description
RoHS	Restriction of Hazardous Substance Directive
China RoHS	Restriction of Hazardous Substance Directive, China

5 References

CF+ and Compact Flash Card Specification Revision 4.1 (for command set only)

6 Part Number Decoder



1. Mfg Process
I: Lead Based
R: RoHS Compliant

2. Technology
F: FLASH (NAND)

3. Form Factor

CF1: Compact Flash 50 pin T-1	DFC3: Discrete Flash Card T-3
CF2: Compact Flash 50 pin T-2	DFC4: Discrete Flash Card T-4
CF1S: Compact Flash C-Fast T-1	~~DUC1: eUSB T-1 Cisco eUSB~~
CF1E: CF with Enhanced ESD	~~DUC2: eUSB T-2 Cisco short eUSB~~
PC1: PC Card 68 pin T-1	DUC3: eUSB T-3 standard profile
PC2: PC Card 68 pin T-2	DUC3L: eUSB T-3 low profile
ID2: IDE Drive 44pin 2.5"	~~DUC4: eUSB T-1 Cisco eUSB+~~
ID3: IDE Drive 40pin 3.5"	CUB1: CUBE^3 T-1 BGA
USB2: USB2 thumbdrive	CUB2: CUBE^3 T-2 µSATA
DOC1: Replaced by DFC1	EC34: ExpressCard 34
DFC1: Discrete Flash Card T-1	EC54: ExpressCard 54
DFC2: Discrete Flash Card T-2	

EP1x: Cisco eUSB Plus, x=firmware version
1 = I0401, 2 = K0509 (Toshiba) or K0526 (Samsung)

4. Capacity

0032: 32MB	0512: 512MB	032G: 32GB
0048: 48MB	0640: 640MB	064G: 64GB
0064: 64MB	1024: 1GB	128G: 128GB
0096: 96MB	2048: 2GB	256G: 256GB
0128: 128MB	4096: 4GB	512G: 512GB
0256: 256MB	8192: 8GB	
0320: 320MB	016G: 16GB	

5. Controller

D: HS F4	N: SM223 (CF)
F: SM221 (CF)	P: SM2242 (SATA)
E: HS F3	R: SM325 (USB)
G: SM232 (PCMCIA)	S: SM2250 (SATA)
H: SM321 (USB)	T: SM233 (PCIe)
J: SM323 (USB)	U: SM2232 (CF)
K: SM222 (CF)	V: SM2234 (CF)
M: SM324 (USB)	W: SM2240 (SATA)
	Y: SMI3252 (USB)

6. Device operating Temperature
C: Commercial (0 to +70 C) I: Industrial (-40 to +85 C)

7. Device Density

1: 128 Mb	7: 4 Gb Mono	N: 64 Gb QDP
2: 256 Mb	E: 8 Gb DDP	P: 128Gb DSP
5: 512 Mb	G : 8 Gb Mono	S: 128 Gb QDP
4: 1 Gb DDP	F: 16 Gb QDP	T: 256 Gb QDP
6: 1 Gb Mono	H : 16 Gb DDP	U: 256 Gb ODP
8: 2 Gb DDP	J: 16Gb Mono	V: 512 Gb ODP
9: 2 Gb Mono	K: 32 Gb QDP	W: 64Gb Mono
X: 2 Gb DST Stack	L: 32 Gb DDP	Y: 128Gb DDP
3: 4 Gb DDP	M: 64 Gb DSP	

DDP = Dual Die Package ; QDP = Quad Die Package

8. Voltage (eUSB)
5: 5V (DUC2 only)
3: 3.3V (DUC1/DUC2/DUC3 only)
blank: industry standard for form factor

OR

8. Firmware version

	SM222A	SM223	SM2232	SM321 SM325	SM3252	HS F3	HS F4
A:	G1120	I1006	J0603	I0401	L0518		091110
B:	J1008		J1206	J1212		100511a	101130
C:			K0927B	J1214		100511d	
D:				K0509		100511e	
E:				K0526			

9. NAND Manufacture
S: Samsung T: Toshiba P: Spansion

10. DRAM die revision:
X: (A, B, C, Etc.)

11. Product variation:
X: (1, 2, 3, Etc.)