MEMORY MODULE SERIAL PRESENCE DETECT (SPD)

Whitepaper

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A RF, Optical, Microelectronics and Memory Company

Abstract

Viking Technology manufactures DRAM modules for OEMs in Enterprise, Telecommunications and Industrial markets. It offers Full DRAM technology portfolio from DDR4 to Legacy DDR1. Viking's modules follow JEDEC standard and range from Standard Form Factors to the most comprehensive small form-factor and Specialty custom modules. For a computer system to recognize a memory module, the module needs to have a chip on it that communicates the specifications of the module to the system. A system's basic input/output system (BIOS) may depend on serial presence detect (SPD) data to properly configure and optimize the memory sub system. Viking's SPD data confirms to JEDEC industry standards and is available through Viking's SPD tool with Viking module part number.

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Serial Presence Detect

1 Serial Presence Detect (SPD)

For a computer system to recognize a memory module, the module needs to have a chip on it that communicates the specifications of the module to the system. If this chip is improperly configured for the system in which you are installing the module, the system won't recognize the memory or may get incorrect information about the module's speed. We can say that in computing, Serial Presence Detect (SPD) is a standardized way to automatically access the information about a memory module. Earlier 72-pin SIMS included five pins that provided five bits of parallel presence data (PPD), but the 168-pin standard changed to a serial presence detect to encode much more information.

Figure-1: Example of SPD

SPD information is written to a single EEPROM that resides on the memory module (DIMM). The pins of the EEPROM are routed to the edge connector of the module so that it may be accessed by the system through the I^2C or SMBus. In this manner, the DIMM's configuration information stays with the module and is accessible by the system the module is installed in.

2 JEDEC Standards

SPD has two basic parts: the hardware, which consists of the EEPROM and the I2C bus on which it resides and the module configuration information that is stored on the EEPROM. JEDEC has defined both the hardware and the data and has documented it in separate sections of JEDEC Standard No. 21C.

This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect
(SPD) standard is intended for use on any memory module, independent of memory technology or module form factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology.

When a specific memory technology is being depicted (e.g., Fast Page Mode DRAM), an annex to this standard will be added describing the characteristics, features, and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each annex.
When a new module form factor implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:

- SPD Interface protocol,
- Acceptable module configurations,
- Legitimate architectures: depth, width, #banks, addressing,
- Acceptable error checking schemes (ECC, Parity...),
- SPD wiring diagram and pinout to module.

Note that all writable memory modules that include a Serial Presence Detect (SPD) feature must also support"Page
Write" operations of at least 4 sequential addresses.

3 SPD Interface protocol

Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Examples of SPD interface protocol include I^2C, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.

The interface standard for the SPD used on all JEDEC memory modules is defined for the following device types:

- EE1002 family of EEPROM devices
- TSE2002 family of EEPROM devices with integrated thermal sensor
- TS3000 family of standalone thermal sensors

Though not technically an SPD device, the TS3000 families of sensors are defined to be compatible with modules using SPD devices. In addition, the TSE2002 family of devices is intended to be a superset of the functionality of EE1002 and TS3000 family devices.

When writing data to the memory, the SPD inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Master generated STOP condition after an Ack for WRITE, and after a NoAck for READ. Violations of the command protocol result in unpredictable operation. The TS section of the device uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/ write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a NoAck and STOP after the Least Significant byte (LSB). Data and address information is transmitted and received starting with the Most Significant Bit first.

3.1 I²C Bus Protocol

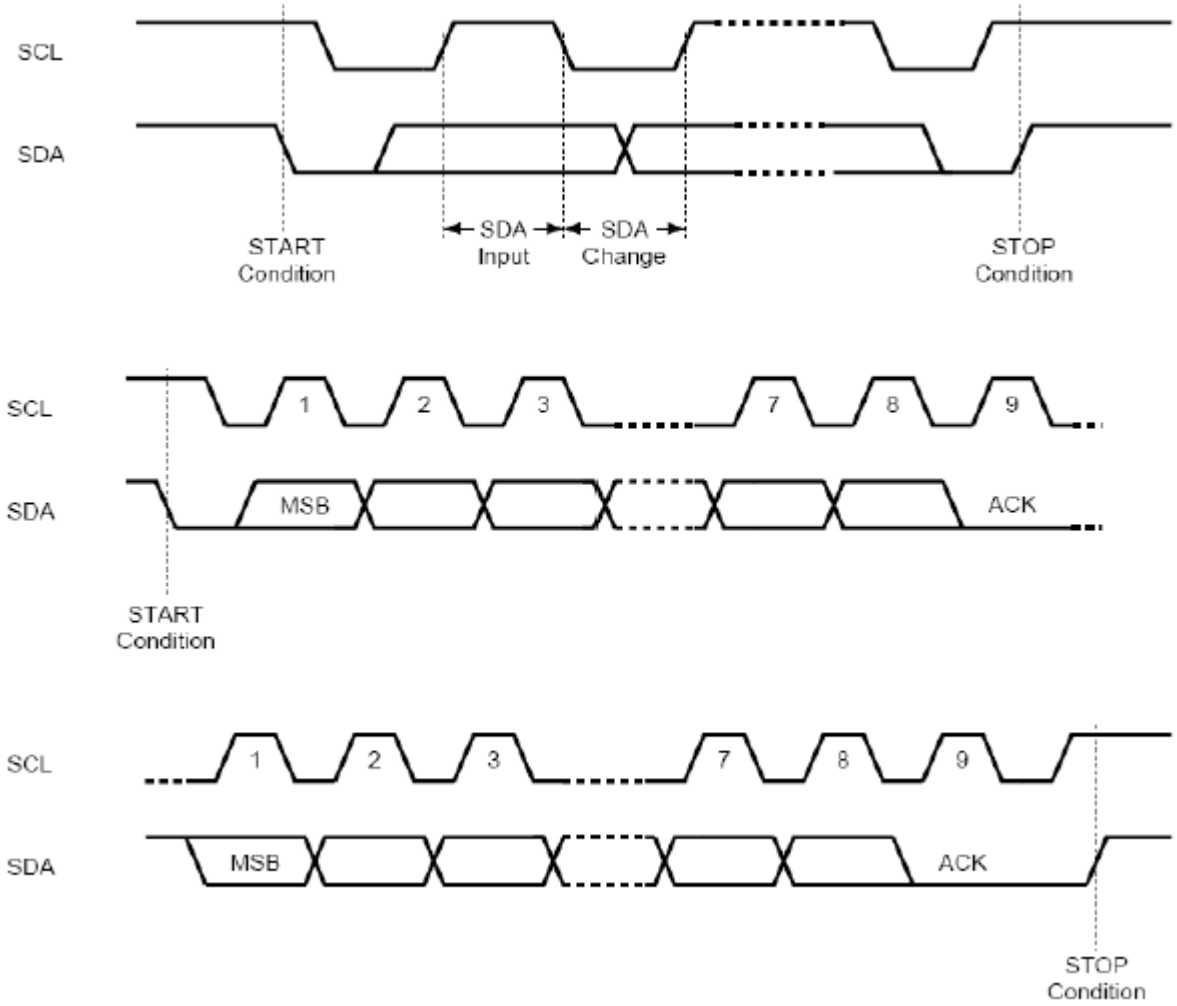

Figure-2 I²C Bus Protocol

3.2 Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

3.3 Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus

master. A Read command that is followed by NoAck can be followed by a Stop condition to force the SPD into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle for the SPD. Neither of these conditions changes the operation of the TS section.

3.3 Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

3.4 No Acknowledge Bit (NACK)

The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus master releases Serial Data (SDA) after sending eight bits of data, and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

3.5 Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven Low.

3.6 Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in the next table (on Serial Data (SDA), most significant bit first).

1.1 4 Data order and PD size

This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required and optional data; when a fundamental memory technology's PD bits are defined, then the entire address map for those SPDs must also be defined.

5 SPD Data Types

SPD data is stored in a non-volatile serial memory device. The different types of data include, but are not limited to:

- Look Up Table entries
- Binary data

- Optional data (Binary, ASCII, etc.)
- Checksums or Cyclic Redundancy Checks

5.1 Look Up Table (LUT) Entries

Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g., fast page mode DRAM will have specific tables for tRAC, tCAC, number of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a lookup table specified within an annex of this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its annexes.

5.2 Optional Data

The current JEDEC Standard allows for manufacturers to insert some of their own specific data into the SPD EEROM. This data includes manufacturer ID, manufacturers' module serial numbers, and other ASCII, Binary Coded Decimal, or binary data.

5.3 Checksums and Cyclic Redundancy Checks

In various cases, checksums are required. This procedure applies to all situations where a Checksum is required.

Checksum calculation method is as follows:
1. Convert binary information in byte locations 0 to 62 to decimal.
2. Sum all decimal values for locations 0 to 62.
3. Divide "sum" by 256.
4. Convert remainder to binary (will be less than 256).
5. Store result (single byte) in location 63 as 'Checksum'.
Note that the same result can be obtained by summing the binary values in locations 0 to 62, and eliminating all but the low order byte. The low order byte would be the 'checksum'.

6 SPD Content, Legacy and Modern Definitions

The legacy SPD definition was traditionally used for memory and module types. As space on the SPD EEPROM ran out, redefinitions of the SPD layout arose for use in subsequent memory and module types. Table-1 summarizes the type of SPD encoding used for various memory types.

Table-1 Legacy and modern definition

Fundamental Memory Type	SPD Encoding
Fast Page Mode (FPM)	Legacy
Extended Data Out (EDO)	Legacy
SDRAM	Legacy
DDR1 SDRAM	Legacy
DDR2 SDRAM except FB-DIMM	Legacy
DDR2 FB-DIMM	DDR2 FB-DIMM
DDR3 SDRAM	DDR3 SDRAM
DDR4 SDRAM	DDR4 SDRAM

Among all the SPD definitions, Byte 2 (Fundamental Memory Type) is the common Key Byte that is used to differentiate the SPD encoding type.

7 EEPROM Function

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to VDDSPD. In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive VDDSPD in the i2C Bus chain.

Select Address (SA0, SA1, SA2)

These input signals are used to create the Logical Serial Address LSA that is compared to the least significant bits (b3, b2, b1) of the 7-bit Slave Address. Refer to the SMBus Address Modes table. The SA0 input is used to detect the VHV voltage, when decoding an SWPn or CWP instruction.

8 Serial Communications

The 4 Kbit serial EEPROM is organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128 byte blocks. The devices are able to selectively lock the data in any or all of the four 128-byte blocks. Designed specifically for use in DRAM

DIMMs (Dual Inline Memory Modules) with Serial Presence Detect, all the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in one or more of the blocks of memory.

The devices used are protocol compatible with previous generation 2 Kbit devices. The page selection method allows commands used with legacy devices to be applied to the lower or upper pages of the current generation devices. In this way, the latest EEPROM may be used in legacy applications without software changes. Minor exceptions to this compatibility, such as elimination of the Permanent Write Protect feature, are documented.

Individually locking a 128-byte block of the SPD may be accomplished using a software write protection mechanism in conjunction with a high input voltage VHV on input SA0. By sending the device a specific SMBus sequence, each block may be protected from writes until write protection is electrically reversed using a separate SMBus sequence which also requires VHV on input SA0. Write protection for all four blocks is cleared simultaneously, and write protection may be reasserted after being cleared.

The Thermal Sensor (TS) section of the device continuously monitors the temperature and updates the temperature data a minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. Finally, the device's EVENT_n pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.

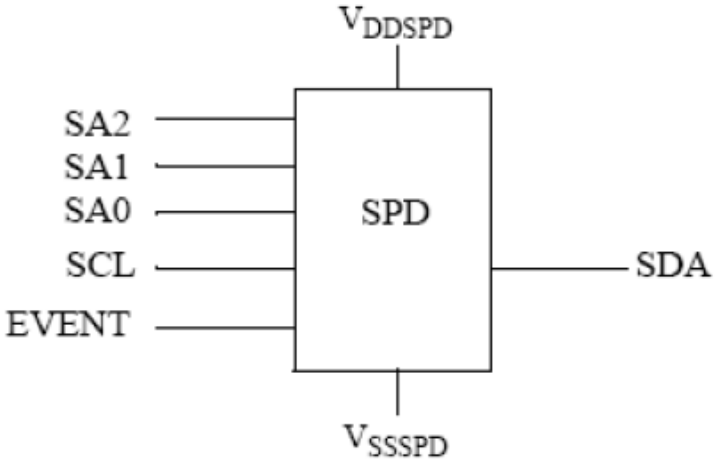

Figure-3 Device Diagram

9 Device Interface

The device behaves as a slave device in the I^2C Bus protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START

condition, generated by the bus master. The START condition is followed by a Device Select Code and R/W# bit (as described in the I2C Bus Operating Mode table), terminated by an acknowledge bit. The device does not initiate clock stretching which is an optional I2C Bus feature.

In accordance with the I2C Bus definition, the device uses three (3) built-in, 4-bit Device Type Identifier Codes (DTIC) and the state of SA0, SA1, and SA2 to generate an I2C Bus Slave Address. The SPD memory may be accessed using a DTIC of (1010), and to perform the SWPn, RSPn, or CSWP operations a DTIC of (0110) is required. The TS registers are accessed using a DTIC of (0011).

10 Serial Address Selections

Inputs SA0, SA1, and SA2 inputs are directly combined with the DTIC and the EE page address bit to qualify SMBus addresses. Each of the SA pins is tied to VDDSPD or VSSSPD and the Logical Serial Address (LSA) is equal to the code on the Serial Address pins.

Table-2 I^2C Bus Addressing Modes

Logical Serial Address (LSA)	SA2	SA1	SA0
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0
101	1	0	1
110	1	1	0
111	1	1	1
Note: 0 = VSSSPD; 1 = VDDSPD			

11 Software Write Protect

The device has three software commands for setting, clearing or interrogating the write-protection status.

Software write-protection is handled by three instructions:
SWPn: Set Write Protection for Block n
CWP: Clear Write Protection for all Blocks
RPSn: Read Protection Status for Block n

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 1

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

11.1 SWPn and CWP: Set and Clear Write Protection

If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears write protection for all blocks.

11.2 Potocol for Write Protection Commands SWPn, CWP, RPSn

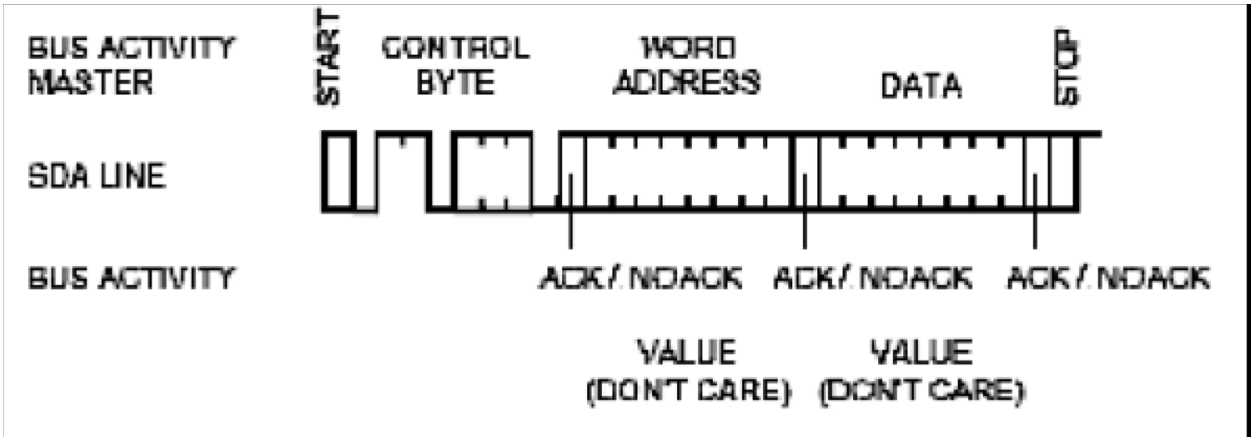

Figure-4 Protocol for Write Protection Commands

11.3 RPSn: Read Protection Status

The controller issues a RPSn command specifying which block to report upon. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck.

11.4 SPAn: Set SPD Page Address

The controller issues an SPAn command to select the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm power-on reset, the SPD Page Address is always 0, selecting the lower 256 bytes.

11.5 RPA: Read SPD Page Address

The controller issues an RPA command to determine if the currently selected SPD page is 0 (device returns Ack) or 1 (device returns NoAck).

12 Write Operations

Following a Start condition the bus master sends a Device Select Code with the R/W_n bit reset to 0. The device acknowledges this and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte. When the bus master generates a Stop condition immediately after the Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle. During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored by the EE, and the EE device does not respond to any requests. Access to the TS portion of the device is permitted during this period. The device has an internal address counter which is incremented each time a byte is written. If a Write operation is performed to a protected block, the internal address counter is not incremented.

12.1 Byte Write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. After the byte is transferred, the internal byte address counter is incremented unless the block is write protected. The bus master terminates the transfer by generating a Stop condition.

12.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion. The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.

12.3 Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (tW) can be obtained from the device’s AC Characteristic table, but the typical time is shorter. To

make use of this, a polling sequence can be used by the bus master. The polling sequence can be performed as follows:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

13 Read Operations

Read operations are performed independent of the software protection state. The device has an internal address counter which is incremented each time a byte is read.

13.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (refer to the Read Mode Sequence figure) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the R/W_n bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

13.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/W_n bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in the Read Mode Sequence figure, without acknowledging the byte.

13.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition (refer to the Read Mode Sequence figure). The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

13.4 Acknowledge in Read Mode

For all Read commands to the SPD, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition. This has no effect on the TS operational status.

14 SPD Common Landing Pattern

The SPD common landing pattern is shown in Figure-4 (JEDEC Standard No. 21C) and its parameters are explained in Table-3 (JEDEC Standard No. 21C). The common landing pattern recommendations for the TDFN packaged SPD (EE1002 compatible) or SPD with Thermal Sensor (TSE2002 compatible) are parameterized to allow for routing design constraints. The preferred implementation with wide corner pads enhances device centering during assembly, but two narrower options are defined for modules with tight routing requirements.

Figure-5 SPD Common Landing Pattern

Parameter	Description	Dimension			Notes
		Min	Nom	Max	
D2	Heat paddle width	1.40	-	1.60	
E2	Heat paddle height	1.40	-	1.60	
E3	Heat paddle centerline to contact inner locus	1.00	-	1.05	
L	Contact length	0.70	-	0.80	
K	Heat paddle to contact keepout	0.20	-	-	
K2	Contact to contact keepout	0.20	-	-	
e	Contact centerline to contact centerline pitch for inner contacts	-	0.50	-	
b	Contact width for inner contacts	0.25	-	0.30	
e2	Landing pattern centerline to outer contact centerline, “minimum acceptable” option	-	0.50	-	1
b2	Corner contact width, “minimum acceptable” option	0.25	-	0.30	1
e3	Inner contact centerline to outer contact centerline, “intermediate” option	-	0.55	-	2
b3	Corner contact width, “intermediate” option	0.35	-	0.40	2
e4	Landing pattern centerline to outer contact centerline, “preferred” option	-	0.60	-	3
b4	Corner contact width, “preferred” option	0.45	-	0.50	3

NOTE 1 Minimum acceptable option to be used when routing prevents preferred or intermediate width contact.
NOTE 2 Intermediate option to be used when routing prevents preferred width contact.
NOTE 3 Preferred option to be used when possible.

Table-3 Parameters for SPD Common Landing Patterns

Global Locations				
US Headquarters	Canada Office	Texas Office	India Office	Singapore Office
2950 Red Hill Ave. Costa Mesa, CA 92626 Main: +1 714 913 2200 Fax: +1 714 913 2202	500 March Road Ottawa, ON K2K 0J9 Canada	1201 W. Crosby Road Carrollton, TX 75006 USA	A 3, Phase II, MEPZ- Special Economic Zone NH 45, Tambaram, Chennai-600045 India	No 2 Chai Chee Drive Singapore, 109840
For all of our global locations, visit our website under global locations. For sales information, email us at sales@vikingtechnology.com				

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A RF, Optical, Microelectronics and Memory Company