

**Module Configuration**

Viking Part Number	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR7UA1G7254GHZ	8GB	1Gx72	512Mx4 (36 die)	TFBGA Stack	2	PC3-6400	CL6 (6-6-6)
VR7UA1G7254GHA	8GB	1Gx72	512Mx4 (36 die)	TFBGA Stack	2	PC3-8500	CL7 (7-7-7)
VR7UA1G7254GHD	8GB	1Gx72	512Mx4 (36 die)	TFBGA Stack	2	PC3-10600	CL9 (9-9-9)
VR7UA1G7254GHx	8GB	1Gx72	512Mx4 (36 die)	TFBGA Stack	2	PC3-12800	CL10 (10-10-10)
VR7UA1G7254GHF	8GB	1Gx72	512Mx4 (36 die)	TFBGA Stack	2	PC3-12800	CL11 (11-11-11)
VR7UA2G7254HHZ	16GB	2Gx72	1024Mx4 (36 die)	TFBGA Stack	2	PC3-6400	CL6 (6-6-6)
VR7UA2G7254HHA	16GB	2Gx72	1024Mx4 (36 die)	TFBGA Stack	2	PC3-8500	CL7 (7-7-7)
VR7UA2G7254HHD	16GB	2Gx72	1024Mx4 (36 die)	TFBGA Stack	2	PC3-10600	CL9 (9-9-9)
VR7UA2G7254HHx	16GB	2Gx72	1024Mx4 (36 die)	TFBGA Stack	2	PC3-12800	CL10 (10-10-10)
VR7UA2G7254HHF	16GB	2Gx72	1024Mx4 (36 die)	TFBGA Stack	2	PC3-12800	CL11 (11-11-11)

For part numbers containing an x, contact Viking for the complete PN

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**Features**

- JEDEC standard Power Supply
  - VDD = VDDQ= 1.5V ±0.075V
- 240-pin Registered Dual-In-Line Memory Module with parity bit for address and control bus.
- 8 Internal Banks.
- Programmable CAS Latency: 6, 7, 8, 9, 10
- Programmable CAS Write Latency (CWL).
- Programmable Additive Latency (Posted CAS).
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh. Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.
- Serial Presence Detect with EEPROM.
- On-DIMM Thermal Sensor.
- Asynchronous Reset.
- ULP RDIMM dimensions: 133.35 mm x 17.75 mm.\
- RoHS Compliant\* (see last page)

**Nomenclature**

Module Standard	SDRAM Standard	Clock
PC3-6400	DDR3-800	400MHz
PC3 -8500	DDR3-1066	533MHz
PC3-10600	DDR3-1333	667MHz
PC3-12800	DDR3-1600	800MHz

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**PIN CONFIGURATIONS**

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VREFDQ	121	VSS	31	DQ25	151	VSS	61	A2	181	A1	91	DQ41	211	VSS
2	VSS	122	DQ4	32	VSS	152	DQS12, TDQS12	62	VDD	182	VDD	92	VSS	212	DQS14, TDQS14
3	DQ0	123	DQ5	33	DQS3#	153	DQS12#, TDQS12#	63	CK1	183	VDD	93	DQS5#	213	DQS14#, TDQS14#
4	DQ1	124	VSS	34	DQS3	154	VSS	64	CK1#	184	CK0	94	DQS5	214	VSS
5	VSS	125	DQS9, TDQS9	35	VSS	155	DQ30	65	VDD	185	CK0#	95	VSS	215	DQ46
6	DQS0#	126	DQS9#, TDQS9#	36	DQ26	156	DQ31	66	VDD	186	VDD	96	DQ42	216	DQ47
7	DQS0	127	VSS	37	DQ27	157	VSS	67	VREFCA	187	EVENT#, NC	97	DQ43	217	VSS
8	VSS	128	DQ6	38	VSS	158	CB4	68	Par_In	188	A0	98	VSS	218	DQ52
9	DQ2	129	DQ7	39	CB0	159	CB5	69	VDD	189	VDD	99	DQ48	219	DQ53
10	DQ3	130	VSS	40	CB1	160	VSS	70	A10 / AP	190	BA1	100	DQ49	220	VSS
11	VSS	131	DQ12	41	VSS	161	DQS17, TDQS17	71	BA0	191	VDD	101	VSS	221	DQS15, TDQS15
12	DQ8	132	DQ13	42	DQS8#	162	DQS17#, TDQS17#	72	VDD	192	RAS#	102	DQS6#	222	DQS15#, TDQS15#
13	DQ9	133	VSS	43	DQS8	163	VSS	73	WE#	193	S0#	103	DQS6	223	VSS
14	VSS	134	DQS10, TDQS10	44	VSS	164	CB6	74	CAS#	194	VDD	104	VSS	224	DQ54
15	DQS1#	135	DQS10#, TDQS10#	45	CB2	165	CB7	75	VDD	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	VSS	46	CB3	166	VSS	76	S1#	196	A13	106	DQ51	226	VSS
17	VSS	137	DQ14	47	VSS	167	NC(TEST)	77	ODT1	197	VDD	107	VSS	227	DQ60
18	DQ10	138	DQ15	48	VTT	168	RESET#	78	VDD	198	S3#	108	DQ56	228	DQ61
19	DQ11	139	VSS	<b>KEY</b>				79	S2#	199	VSS	109	DQ57	229	VSS
20	VSS	140	DQ20	49	VTT	169	CKE1	80	VSS	200	DQ36	110	VSS	230	DQS16, TDQS16
21	DQ16	141	DQ21	50	CKE0	170	VDD	81	DQ32	201	DQ37	111	DQS7#	231	DQS16#, TDQS16#
22	DQ17	142	VSS	51	VDD	171	A15	82	DQ33	202	VSS	112	DQS7	232	VSS
23	VSS	143	DQS11, TDQS11	52	BA2	172	A14	83	VSS	203	DQS13, TDQS13	113	VSS	233	DQ62
24	DQS2#	144	DQS11#, TDQS11#	53	Err_Out#	173	VDD	84	DQS4#	204	DQS13#, TDQS13#	114	DQ58	234	DQ63
25	DQS2	145	VSS	54	VDD	174	A12 / BC#	85	DQS4	205	VSS	115	DQ59	235	VSS
26	VSS	146	DQ22	55	A11	175	A9	86	VSS	206	DQ38	116	VSS	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	VDD	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	VSS	57	VDD	177	A8	88	DQ35	208	VSS	118	SCL	238	SDA
29	VSS	149	DQ28	58	A5	178	A6	89	VSS	209	DQ44	119	SA2	239	VSS
30	DQ24	150	DQ29	59	A4	179	VDD	90	DQ40	210	DQ45	120	VTT	240	VTT
				60	VDD	180	A3								

**PIN FUNCTION DESCRIPTION**

SYMBOL	TYPE	POLARITY	DESCRIPTION
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.

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**PIN FUNCTION DESCRIPTION**

SYMBOL	TYPE	POLARITY	DESCRIPTION
/CK0	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[3:0]#	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both S[1:0] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, S[3:2] operate similarly to S[1:0] for a second set of register outputs.
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS#, CAS#, WE#	IN	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operation to be executed by the SDRAM.
VREFDQ	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
VREFCA	Supply		Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S1#, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	-	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during a MRS cycle.
A[15:13, 12/BC, 11, 10/AP, 9:0]	IN	-	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during CAS# command. The address inputs also provide the op-code during Mode Register Set commands.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input/Output pins
VDD, VSS	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
DM [8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
VDD, VSS	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
VTT	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS [17:0]#	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
TDQS[17:9], TDQS[17:9]#	OUT		TDQS, TDQS# is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS, TDQS# that is applied to DQS, DQS#. When disabled via mode register A11=0 in MR1, DM, TDQS will provide the data mask function and TDQS# is not used. X4/X16 DRAMs must disable the TDQS function via mode register A11=0 in MR1
SA [2:0]	IN	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDDSPD on the system planar to act as a pull-up.
EVENT#	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT pin on TS/SPD part.

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**PIN FUNCTION DESCRIPTION**

SYMBOL	TYPE	POLARITY	DESCRIPTION
VDDSPD	Supply	-	Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET#	IN		The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus. ("1 ": Odd, "0 ": Even)
Err_Out#	OUT		Parity error found in the Address and Control bus
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

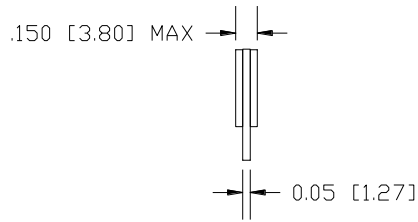
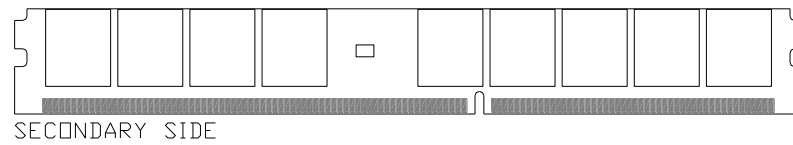
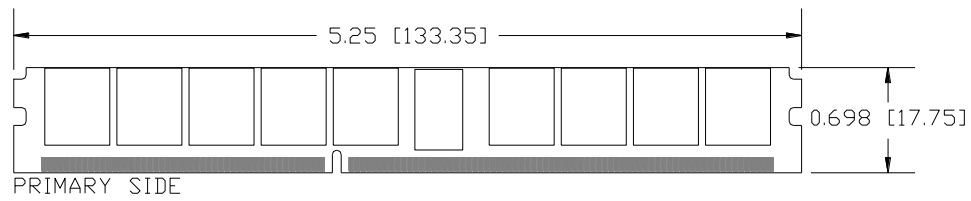
**MECHANICAL OUTLINE**

Dimensions are in inches. (Tolerance is +/- 0.005, unless otherwise stated.)

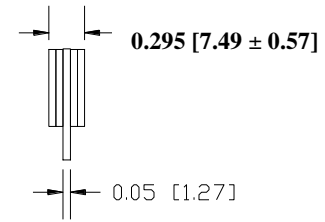
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SINGLE RANK

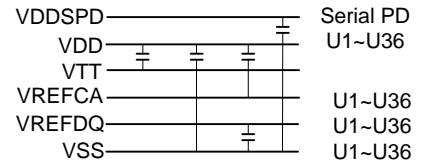
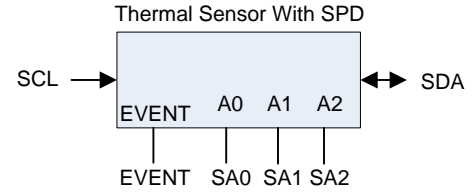
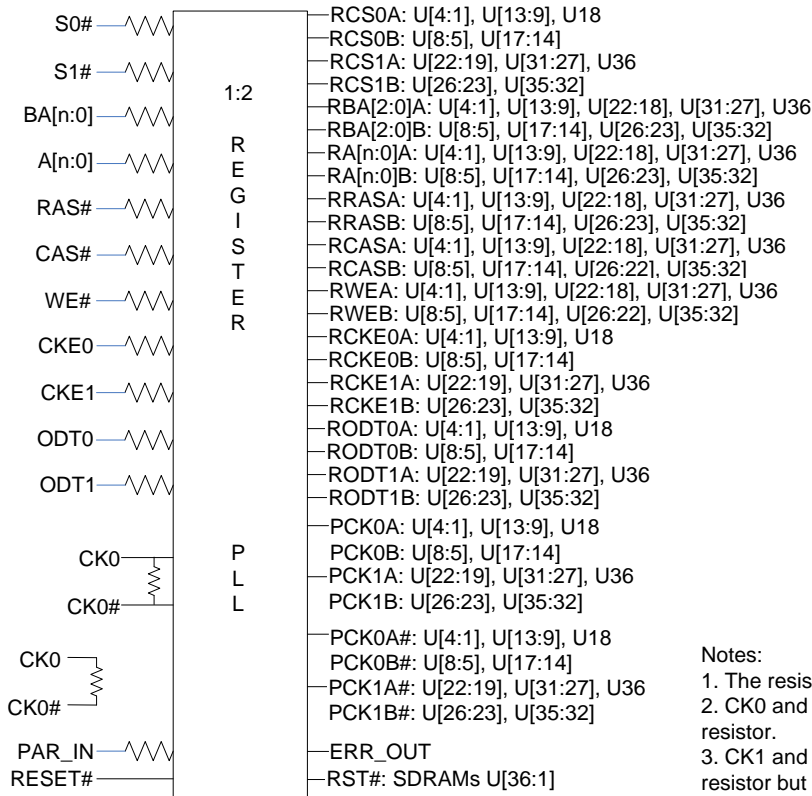


BGA STACK DUAL RANK

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**FUNCTIONAL BLOCK DIAGRAM**



**Notes:**

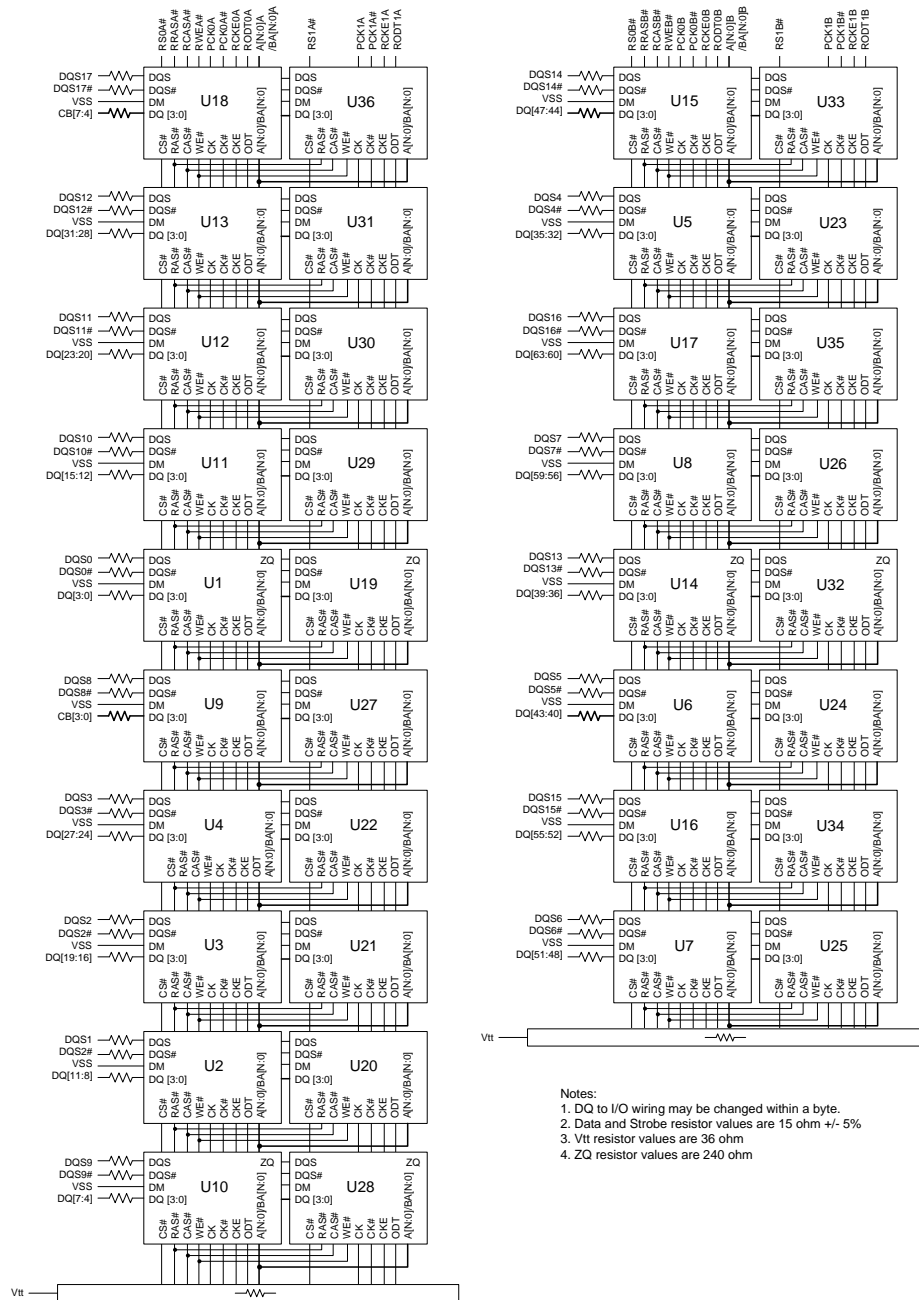
1. The resistor values may vary depending on systems application
2. CK0 and CK0# are differentially terminated with single 120Ω resistor.
3. CK1 and CK1# are differentially terminated with single 120Ω resistor but is not used.

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FUNCTIONAL BLOCK DIAGRAM



- Notes:
1. DQ to I/O wiring may be changed within a byte.
  2. Data and Strobe resistor values are 15 ohm +/- 5%
  3. Vtt resistor values are 36 ohm
  4. ZQ resistor values are 240 ohm

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### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND	Vin, Vout	-0.4 ~ 1.975	V
Voltage on VDD supply relative to GND	VDD	-0.4 ~ 1.975	V
Voltage on VDDQ supply relative to GND	VDDQ	-0.4 ~ 1.975	V
Storage temperature	TSTG	-55 ~ +100	°C

**Note:** Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

### DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL\_1.5)

Recommended operating conditions (Voltages referenced to GND, Tcase = 0 to 85°C)

Parameter	Symbol	Min.	Max.	Unit	Notes
Case Temperature	Tcase	0	95	°C	5
Supply voltage	VDD	1.425	1.575	V	1, 2
Supply voltage for DQ, DQS	VDDQ	1.425	1.575	V	1, 2
Reference Voltage for DQ, DM inputs	VREFDQ(DC)	0.49 x VDD	0.51 x VDD	V	3, 4
Reference Voltage for ADD, CMD inputs	VREFCA(DC)	0.49 x VDD	0.51 x VDD	V	3, 4
Terminal Voltage	VTT	0.49 x VDD	0.51 x VDD	V	3, 4
EEPROM Supply Voltage	VDDSPD	1.7	3.6	V	
Input high voltage	VIH(AC)	VREF + 0.175	-	V	
	VIH(DC)	VREF + 0.100	VDD		
Input low voltage	VIL(AC)	-	VREF - 0.175	V	
	VIL(DC)	VSS	VREF - 0.100		
Input leakage current	Single Rank	IIL	-5	5	µA
Output leakage current	Single Rank	IOL	-5	5	µA
Input leakage current	Dual Rank	IIL	-5	5	µA
Output leakage current	Dual Rank	IOL	-10	10	µA

- Note:**
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together
  - Under all conditions VDDQ must be less than or equal to VDD.
  - The ac peak noise on VREF may not allow VREF to deviate from VREF.DC by more than ±1% VDD (for reference: approx. ± 15 mV).
  - For reference: approx. VDD/2 ± 15 mV.
  - Refresh rate required to be doubled (tREFI = 3.9µs) when 85°C < TC < 95°C.

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**DEVICE CAPACITANCE**

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS,TDQS#)	CIO	1.5	3.0	1.5	2.7	1.5	2.5	pF	1,2,3
Input capacitance, CK and CK#	CCK	0.8	1.6	0.8	1.6	0.8	1.4	pF	2,3
Input capacitance delta, CK and CK#	CDCK	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input/output capacitance delta DQS and DQS#	CDDQS	0	0.2	0	0.2	0	0.15	pF	2,3,5
Input capacitance, (CTRL, ADD, CMD input-only pins)	CI	0.75	1.4	0.75	1.35	0.75	1.3	pF	2,3,6
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	pF	2,3,7

**DEVICE CAPACITANCE (Cont.)**

Parameter	Symbol	DDR3-1600		DDR3-1866		Min	Max	Units	Notes
		Min	Max	Min	Max				
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS,TDQS#)	CIO	1.5	2.3	1.4	2.2			pF	1,2,3
Input capacitance, CK and CK#	CCK	0.8	1.4	0.8	1.3			pF	2,3
Input capacitance delta, CK and CK#	CDCK	0	0.15	0	0.15			pF	2,3,4
Input/output capacitance delta DQS and DQS#	CDDQS	0	0.15	0	0.15			pF	2,3,5
Input capacitance, (CTRL, ADD, CMD input-only pins)	CI	0.75	1.3	0.75	1.2			pF	2,3,6
Input/output capacitance of ZQ pin	CZQ	-	3	-	3			pF	2,3,7

**Note:**

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of CCK-CCK#
5. Absolute value of CIO(DQS)-CIO(DQS#)
6. CI applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. Maximum external load capacitance on ZQ pin: 5 pF.

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**IDD DC CHARACTERISTICS DEFINITIONS (Recommended operating conditions unless otherwise noted, Tcase = 0 to 85 °C)**

Symbol	Conditions	Units	Notes
IDD0	<b>Operating one bank active-precharge current;</b> tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2
IDD1	<b>Operating one bank active-read-precharge current;</b> IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2
IDD2P-S	<b>Precharge power-down current (slow exit);</b> All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2P-F	<b>Precharge power-down current (fast exit);</b> All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2Q	<b>Precharge quiet standby current;</b> All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2N	<b>Precharge standby current;</b> All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD3P	<b>Active power-down current;</b> All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD3N	<b>Active standby current;</b> All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD4W	<b>Operating burst write current;</b> All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2
IDD4R	<b>Operating burst read current;</b> All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2
IDD5B	<b>Burst refresh current;</b> tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD6	<b>Self refresh current;</b> CK and CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	mA	1, 3
IDD6ET	<b>Extended Temperature Range Self-Refresh Current;</b> CK and CK at 0V; CKE ≤ 0.2V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6=0 and A7=1	mA	1, 3
IDD7	<b>Operating bank interleave read current;</b> All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	mA	1, 2

**Notes:**

1. Calculated values are from component data.
2. One module rank in the active IDD; the other rank in IDD2P-S (slow exit)
3. All ranks in this IDD condition.

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**IDD**  
**DC CHARACTERISTICS CURRENTS DUAL RANK 2Gbit**  
**Estimated values only**

Symbol	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Unit
IDD0	1350	1710	1890	2033	mA
IDD1	1890	2160	2430	2596	mA
IDD2P-S	360	360	360	385	mA
IDD2P-F	900	900	900	1008	mA
IDD2Q	1800	2160	2520	2777	mA
IDD2N	1800	2160	2520	2646	mA
IDD3P	1620	1800	2160	2393	mA
IDD3N	2340	2700	3240	3504	mA
IDD4R	3240	3690	4230	4678	mA
IDD4W	3600	4140	4680	5010	mA
IDD5B	9900	10440	10980	11678	mA
IDD6	324	324	324	346	mA
IDD6ET	432	432	432	432	mA
IDD7	5850	6300	7560	7836	mA

**DC CHARACTERISTICS CURRENTS DUAL RANK 4Gbit (Hynix A die)**

Symbol	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Unit	Notes
IDD0	1041	1060	1879	2106	mA	1,2,5,6
IDD1	1197	1228	2011	2257	mA	1,2,5,6
IDD2P-S	360	360	655	655	mA	1,2,5,6
IDD2P-F	487	513	730	730	mA	1,2,5,6
IDD2Q	734	718	1596	1633	mA	1,2,5,6
IDD2N	721	738	1558	1596	mA	1,2,5,6
IDD3P	900	900	995	1033	mA	1,2,5,6
IDD3N	814	830	1898	1974	mA	1,2,5,6
IDD4R	2025	2218	2786	3183	mA	1,2,5,6
IDD4W	1735	1895	2881	3278	mA	1,2,5,6
IDD5B	3662	3676	4960	5168	mA	1,2,5,6
IDD6	396	396	806	806	mA	1,2,3,5,6
IDD6ET	504	504	957	957	mA	2,4,5,6
IDD7	3432	3602	3920	4223	mA	1,2,5,6

**Notes:**

1. T<sub>c</sub> = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase IDD<sub>x</sub> by up to an additional 2mA.
3. Restricted to TC (MAX) = 85°C.
4. T<sub>c</sub> = 85°C; ASR and ODT are disabled; SRT is enabled.
5. The IDD values must be derated (increased) on IT-option devices when operated outside of the range 0°C ≤ T<sub>c</sub> ≤ +85°C:
  - 5a: When T<sub>c</sub> < 0°C: IDD2P0, IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD4W must be derated by 2%; and IDD6, IDD6ET and IDD7 must be derated by 7%.
  - 5b: When T<sub>c</sub> > 85°C: IDD0, IDD1, IDD2N, IDD2NT, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; IDD2Px must be derated by 30%.
6. IDD calculations based on DRAM device IDD spec x 18 DRAM per rank (Hynix A-die)

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## REGISTERING CLOCK DRIVER SPECIFICATIONS

SSTE82882 or equivalent

Symbol	Parameter	Pins	Min	Nom	Max	Units
VDD	DC supply voltage	–	1.425	1.5	1.575	V
VREF	DC reference voltage	–	$0.49 \times VDD$	$0.5 \times VDD$	$0.51 \times VDD$	V
VTT	DC termination voltage	–	$VREF - 40 \text{ mV}$	VREF	$VREF + 40 \text{ mV}$	V
VIH(AC)	AC high-level input voltage	Control, command, address	$VREF + 175\text{mV}$	–	$VDD + 0.4$	V
VIL(AC)	AC low-level input voltage	Control, command, address	-0.4	–	$VREF - 175\text{mV}$	V
VIH(DC)	DC high-level input voltage	Control, command, address	$VREF + 100\text{mV}$	–	$VDD + 0.4$	V
VIL(DC)	DC low-level input voltage	Control, command, address	-0.4	–	$VREF - 100\text{mV}$	V
VIH (CMOS)	High-level input voltage	RESET#, MIRROR	$0.65 \times VDD$	–	VDD	V
VIL (CMOS)	Low-level input voltage	RESET#, MIRROR	0	–	$0.35 \times VDD$	V
VIX(AC)	Differential input crosspoint voltage range	CK, CK#, FBIN, FBIN#	$0.5 \times VDD - 175\text{mV}$	$0.5 \times VDD$	$0.5 \times VDD + 175\text{mV}$	V
VID(AC)	Differential input voltage	CK, CK#	350	–	$VDD + \text{TBD}$	mV
IOH	High-level output current	FBOUT, FBOUT#	–	–	11	mA
IOL	Low-level output current	ERR_OUT#	25	28	TBD	mA

**Notes:** Timing and switching specifications for the register are critical for proper operation of the DDR3 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module.

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## AC CHARACTERISTICS

### Refresh parameters by device density

Parameter	Symbol	1Gb	2Gb	4Gb	8Gb	Units	Notes	
REF command to ACT or REF command time	tRFC	110	160	260	350	ns		
Average periodic refresh interval	tREFI	0 °C ≤ TCASE ≤ 85 °C	7.8	7.8	7.8	7.8	µs	
		85 °C < TCASE ≤ 95 °C	3.9	3.9	3.9	3.9	µs	1

**Note:** 1) Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

### DDR3-800 Speed Bins and Operating Conditions

Speed Bin		DDR3-800		Unit	Notes	
CL-nRCD-nRP		6-6-6				
Parameter	Symbol	min	max			
Internal read command to first data	tAA	15	20	ns		
ACT to internal read or write delay time	tRCD	15	—	ns		
PRE command period	tRP	15	—	ns		
ACT to ACT or REF command period	tRC	52.5	—	ns		
ACT to PRE command period	tRAS	37.5	9 * tREFI	ns		
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1, 2, 3
Supported CL Settings		6		nCK	13	
Supported CWL Settings		5		nCK		

### DDR3-1066 Speed Bins and Operating Conditions

Speed Bin		DDR3-1066		Unit	Note	
CL-nRCD-nRP		7-7-7				
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.125	20	ns		
ACT to internal read or write delay time	tRCD	13.125	—	ns		
PRE command period	tRP	13.125	—	ns		
ACT to ACT or REF command period	tRC	50.625	—	ns		
ACT to PRE command period	tRAS	37.5	9 * tREFI	ns		
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,6,
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4,
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,4,
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4,
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,
Supported CL Settings		6, 7, 8		nCK	13	
Supported CWL Settings		5, 6		nCK		

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**DDR3-1333 Speed Bins and Operating Conditions**

Speed Bin		DDR3-1333		Unit	Note	
CL-nRCD-nRP		9-9-9				
Parameter	Symbol	min	max			
Internal read command to first data	<i>tAA</i>	13.5 (13.125)5,11	20	ns		
ACT to internal read or write delay time	<i>tRCD</i>	13.5 (13.125)5,11	—	ns		
PRE command period	<i>tRP</i>	13.5 (13.125)5,11	—	ns		
ACT to ACT or REF command period	<i>tRC</i>	49.5 (49.125)5,11	—	ns		
ACT to PRE command period	<i>tRAS</i>	36	9 * tREFI	ns		
CL = 6	CWL = 5	<i>tCK(AVG)</i>	2.5	3.3	ns	1,2,3,7
	CWL = 6	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4,7
	CWL = 7	<i>tCK(AVG)</i>	Reserved		ns	4
CL = 7	CWL = 5	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 6	<i>tCK(AVG)</i>	1.875	< 2.5	ns	1,2,3,4,7
			(Optional)5,11			
CWL = 7	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4	
CL = 8	CWL = 5	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 6	<i>tCK(AVG)</i>	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 7	<i>tCK(AVG)</i>	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 7	<i>tCK(AVG)</i>	1.5	<1.875	ns	1,2,3
			(Optional)			
Supported CL Settings		6, 8, (7), 9, (10)		<i>nCK</i>		
Supported CWL Settings		5, 6, 7		<i>nCK</i>		

**DDR3-1600 Speed Bins and Operating Conditions**

Speed Bin		DDR3-1600		Unit	Note	
CL-nRCD-nRP		11-11-11				
Parameter	Symbol	min	max			
Internal read command to first data	<i>tAA</i>	13.75 (13.125)9	20	ns		
ACT to internal read or write delay time	<i>tRCD</i>	13.75 (13.125)9	—	ns		
PRE command period	<i>tRP</i>	13.75 (13.125)9	—	ns		
ACT to ACT or REF command period	<i>tRC</i>	48.75 (48.125)9	—	ns		
ACT to PRE command period	<i>tRAS</i>	35	9 * tREFI	ns		
CL = 6	CWL = 5	<i>tCK(AVG)</i>	2.5	3.3	ns	1,2,3,7
	CWL = 6	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4,7
	CWL = 7	<i>tCK(AVG)</i>	Reserved		ns	4
CL = 7	CWL = 5	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 6	<i>tCK(AVG)</i>	1.875	< 2.5	ns	1,2,3,4,7
			(Optional)5,11			
CWL = 7	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4	
CL = 8	CWL = 5	<i>tCK(AVG)</i>	Reserved		ns	4

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Speed Bin		DDR3-1600		Unit	Note	
CL-nRCD-nRP		11-11-11				
Parameter	Symbol	min	max			
CL = 9	CWL = 6	<i>tCK(AVG)</i>	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4
	CWL = 5, 6	<i>tCK(AVG)</i>	Reserved		ns	4
CL = 10	CWL = 7	<i>tCK(AVG)</i>	1.5	<1.875	ns	1,2,3,4
	CWL = 5, 6	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 7	<i>tCK(AVG)</i>	1.5	<1.875	ns	1,2,3
CL = 11	CWL = 5, 6, 7	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 8	<i>tCK(AVG)</i>	1.25	<1.5	ns	1,2,3,9
Supported CL Settings		6, 8, 7, 9, 10, 11		<i>nCK</i>		
Supported CWL Settings		5, 6, 7, 8		<i>nCK</i>		

**DDR3-1866 Speed Bins and Operating Conditions**

Speed Bin		DDR3-1866		Unit	Note	
CL-nRCD-nRP		13-13-13				
Parameter	Symbol	min	max			
Internal read command to first data	<i>tAA</i>	13.91 (13.125)10	20	ns		
ACT to internal read or write delay time	<i>tRCD</i>	13.91 (13.125)10	—	ns		
PRE command period	<i>tRP</i>	13.91 (13.125)10	—	ns		
ACT to ACT or REF command period	<i>tRC</i>	47.91 (48.125)10	—	ns		
ACT to PRE command period	<i>tRAS</i>	34	9 * tREFI	ns		
CL = 6	CWL = 5	<i>tCK(AVG)</i>	2.5	3.3	ns	1,2,3,8
	CWL = 6	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4,8
	CWL = 7,8,9	<i>tCK(AVG)</i>	Reserved		ns	4
CL = 7	CWL = 5	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 6	<i>tCK(AVG)</i>	1.875	2.5	ns	1,2,3,4,8
	CWL = 7,8,9	<i>tCK(AVG)</i>	(Optional)5, 11		ns	1,2,3,4
CL = 8	CWL = 5	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 6	<i>tCK(AVG)</i>	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4,8
	CWL = 8,9	<i>tCK(AVG)</i>	Reserved		ns	4
CL = 9	CWL = 5,6	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 7	<i>tCK(AVG)</i>	1.5	1.875	ns	1,2,3,4,8
	CWL = 8	<i>tCK(AVG)</i>	Reserved		ns	4
CL = 10	CWL = 5,6,7	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 7	<i>tCK(AVG)</i>	1.5	<1.875	ns	1,2,3,8
	CWL = 8	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4,8
CL = 11	CWL = 5,6,7	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 8	<i>tCK(AVG)</i>	1.25	1.5	ns	1,2,3,8
	CWL = 9	<i>tCK(AVG)</i>	Reserved		ns	1,2,3,4

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Speed Bin			DDR3-1866		Unit	Note
CL-nRCD-nRP			13-13-13			
Parameter	Symbol	min	max			
CL = 12	CWL = 5, 6, 7,8	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 9	<i>tCK(AVG)</i>	1.25	<1.5	ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	<i>tCK(AVG)</i>	Reserved		ns	4
	CWL = 9	<i>tCK(AVG)</i>	1.071	<1.25	ns	1,2,3,9
Supported CL Settings			6, 8, 7, 9, 10, 11,13		<i>nCK</i>	
Supported CWL Settings			5, 6, 7, 8, 9		<i>nCK</i>	

**Notes:**

1. Absolute Specification (TOPER; VDDQ = VDD = 1.5V +/- 0.075 V);
2. The CL setting and CWL setting result in *tCK(AVG)*.MIN and *tCK(AVG)*.MAX requirements. When making a selection of *tCK(AVG)*, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
3. *tCK(AVG)*.MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard *tCK(AVG)* value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07, or 0.935 ns) when calculating CL [*nCK*] = *tAA* [ns] / *tCK(AVG)* [ns], rounding up to the next 'Supported CL', where *tCK(AVG)* = 3.0 ns should only be used for CL = 5 calculation.
4. *tCK(AVG)*.MAX limits: Calculate *tCK(AVG)* = *tAA*.MAX / CL SELECTED and round the resulting *tCK(AVG)* down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.935 ns). This result is *tCK(AVG)*.MAX corresponding to CL SELECTED.
5. 'Reserved' settings are not allowed. User must program a different value.
6. 'Optional' settings allow certain devices in the industry to support this setting; however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
7. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. For devices supporting optional down binning to CL=7 and CL=9, *tAA*/*tRCD*/*tRP*min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for *tAA*min (Byte 16), *tRCD*min (Byte 18), and *tRP*min (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1066F should program 13.125 ns in SPD bytes for *tAA*min (Byte 16), *tRCD*min (Byte 18), and *tRP*min (Byte 20). Once *tRP* (Byte 20) is programmed to 13.125ns, *tRC*min (Byte 21, 23) also should be programmed accordingly. For example, 49.125ns (*tRAS*min + *tRP*min = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (*tRAS*min + *tRP*min = 35 ns + 13.125 ns) for DDR3-1600K.

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Timing Parameters

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Note	
		MIN	MAX	MIN	MAX	MIN	MAX			
<b>Clock Timing</b>										
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OF F)	8	-	8	-	8	-	ns	6	
Average Clock Period	tCK(avg)	See Speed Bins Table						ps		
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps		
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)		
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)		
Clock Period Jitter	tJIT(per)	-100	100	-90	90	-80	80	ps		
Clock Period Jitter during DLL locking period	tJIT(per, ick)	-90	90	-80	80	-70	70	ps		
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160		ps		
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, ick)	180		160		140		ps		
Cumulative error across 2 cycles	tERR(2per)	-147	147	-132	132	-118	118	ps		
Cumulative error across 3 cycles	tERR(3per)	-175	175	-157	157	-140	140	ps		
Cumulative error across 4 cycles	tERR(4per)	-194	194	-175	175	-155	155	ps		
Cumulative error across 5 cycles	tERR(5per)	-209	209	-188	188	-168	168	ps		
Cumulative error across 6 cycles	tERR(6per)	-222	222	-200	200	-177	177	ps		
Cumulative error across 7 cycles	tERR(7per)	-232	232	-209	209	-186	186	ps		
Cumulative error across 8 cycles	tERR(8per)	-241	241	-217	217	-193	193	ps		
Cumulative error across 9 cycles	tERR(9per)	-249	249	-224	224	-200	200	ps		
Cumulative error across 10 cycles	tERR(10per)	-257	257	-231	231	-205	205	ps		
Cumulative error across 11 cycles	tERR(11per)	-263	263	-237	237	-210	210	ps		
Cumulative error across 12 cycles	tERR(12per)	-269	269	-242	242	-215	215	ps		
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max						ps	24	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25	
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26	
<b>Data Timing</b>										
DQS, DQS to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	ps	13	
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g	
DQ low-impedance time from CK, CK	tLZ(DQ)	-800	400	-600	300	-500	250	ps	13,14, f	
DQ high-impedance time from CK, CK	tHZ(DQ)	-	400	-	300	-	250	ps	13,14, f	
Data setup time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDS(base)	75	-	25	-	30	-	ps	d, 17	
Data hold time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDH(base)	150	-	100	-	65	-	ps	d, 17	
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	ps	28	
<b>Data Strobe Timing</b>										
DQS, DQS READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	tCK	13, 19, g	
DQS, DQS differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	tCK	11, 13, b	
DQS, DQS output high time	tQSH	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g	
DQS, DQS output low time	tQSL	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g	
DQS, DQS WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK		
DQS, DQS WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK		
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-400	400	-300	300	-255	255	ps	13, f	
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-800	400	-600	300	-500	250	ps	13,14, f	
DQS, DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	400	-	300	-	250	ps	12,13,14	
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	29, 31	
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30, 31	
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)	c	
DQS, DQS falling edge setup time to CK, CK rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32	
DQS, DQS falling edge hold time to CK, CK rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32	

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**Timing Parameters (Cont.)**

Speed Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Note	
		MIN	MAX	MIN	MAX	MIN	MAX			
<b>Command and Address Timing</b>										
DLL locking time	tDLLK	512	-	512	-	512	-	nCK		
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e	
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e,18	
WRITE recovery time	tWR	15	-	15	-	15	-	ns	e	
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK		
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-	max (12nCK,15ns)	-			
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK		
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))							nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	22	
ACTIVE to PRECHARGE command period	tRAS	See 13.3 " Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin" on page 37							ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-	max (4nCK,6ns)	-		e	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-		e	
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	ns	e	
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	ns	e	
Command and Address setup time to CK, CK referenced to VIH(AC) / VIL(AC) levels	tIS(base)	200	-	125	-	65	-	ps	b,16	
Command and Address hold time from CK, CK referenced to VIH(AC) / VIL(AC) levels	tIH(base)	275	-	200	-	140	-	ps	b,16	
Command and Address setup time to CK, CK referenced to VIH(AC) / VIL(AC) levels	tIS(base) AC150	200 + 150	-	125 + 150	-	65+125	-	ps	b,16,27	
Control & Address Input pulse width for each input	tIPW	900	-	780	-	620	-	ps	28	
<b>Calibration Timing</b>										
Power-up and RESET calibration time	tZQinitl	512	-	512	-	512	-	nCK		
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK		
Normal operation short calibration time	tZQCS	64	-	64	-	64	-	nCK	23	
<b>Reset Timing</b>										
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-			
<b>Self Refresh Timing</b>										
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-			
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-			

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**Timing Parameters(Cont.)**

Speed	Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Note
			MIN	MAX	MIN	MAX	MIN	MAX		
<b>Power Down Timing</b>										
	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK, 6ns)	-		
	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
	CKE minimum pulse width	tCKE	max (3nCK, 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-		
	Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
	Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK	15
	Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	20
	Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	20
	Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-		
	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	nCK	9
	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	nCK	10
	Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	nCK	9
	Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	nCK	10
	Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-		20,21
	Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
<b>ODT Timing</b>										
	ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
	ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	ns	
	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns	
	ODT turn-on	tAON	-400	400	-300	300	-250	250	ps	7,f
	RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
	RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
<b>Write Leveling Timing</b>										
	First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK	3
	DQS/DQS delay after tDQSS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK	3
	Setup time for tDQSS latch	tWLS	325	-	245	-	195	-	ps	
	Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	325	-	245	-	195	-	ps	
	Write leveling output delay	tWLO	0	9	0	9	0	9	ns	
	Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

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**Timing Parameters(Cont.)**

Speed		DDR3-1600		DDR3-1866		MIN	MAX	Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
<b>Clock Timing</b>									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OF F)	8	-	8	-			ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table						ps	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max			ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53			tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53			tCK(avg)	
Clock Period Jitter	tJIT(per)	-70	70	-60	60			ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-50	50			ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140		120				ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		100				ps	
Cumulative error across 2 cycles	tERR(2per)	- 103	103	- 88	88			ps	
Cumulative error across 3 cycles	tERR(3per)	- 122	122	- 105	105			ps	
Cumulative error across 4 cycles	tERR(4per)	- 136	136	- 117	117			ps	
Cumulative error across 5 cycles	tERR(5per)	- 147	147	- 126	126			ps	
Cumulative error across 6 cycles	tERR(6per)	- 155	155	- 133	133			ps	
Cumulative error across 7 cycles	tERR(7per)	- 163	163	- 139	139			ps	
Cumulative error across 8 cycles	tERR(8per)	- 169	169	- 145	145			ps	
Cumulative error across 9 cycles	tERR(9per)	- 175	175	- 150	150			ps	
Cumulative error across 10 cycles	tERR(10per)	- 180	180	- 154	154			ps	
Cumulative error across 11 cycles	tERR(11per)	- 184	184	- 158	158			ps	
Cumulative error across 12 cycles	tERR(12per)	- 188	188	- 161	161			ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	$tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min$ $tERR(nper)max = (1 - 0.68ln(n))*tJIT(per)max$						ps	24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-			tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-			tCK(avg)	26
<b>Data Timing</b>									
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	100	-	85			ps	13
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-			tCK(avg)	13, g
DQ low-impedance time from CK, CK	tLZ(DQ)	-450	225	-390	195			ps	13,14, f
DQ high-impedance time from CK, CK	tHZ(DQ)	-	225	-	195			ps	13,14, f
Data setup time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDS(base)	10	-	-	-			ps	d, 17
Data hold time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDH(base)	-	-	0	-			ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	360	-	320	-			ps	28
<b>Data Strobe Timing</b>									
DQS, DQS READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19			tCK	13, 19, g
DQS, DQS differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11			tCK	11, 13, b
DQS, DQS output high time	tQSH	0.4	-	0.4	-			tCK(avg)	13, g
DQS, DQS output low time	tQSL	0.4	-	0.4	-			tCK(avg)	13, g
DQS, DQS WRITE Preamble	tWPRE	0.9	-	0.9	-			tCK	
DQS, DQS WRITE Postamble	tWPST	0.3	-	0.3	-			tCK	
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-225	225	-195	195			ps	13,f
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195			ps	13,14,f
DQS, DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195			ps	12,13,14
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55			tCK	29, 31
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55			tCK	30, 31
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.27	0.27	-0.27	0.27			tCK(avg)	c
DQS,DQS falling edge setup time to CK, CK rising edge	tDSS	0.9	Note 19	0.18	-			tCK(avg)	c, 32
DQS,DQS falling edge hold time to CK, CK rising edge	tDSH	0.3	Note 11	0.18	-			tCK(avg)	c, 32

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### 18.1 Jitter Notes

1. Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.
2. These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
3. These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)) crossing to its respective clock signal (CK, CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
4. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing. Specific Note e For these parameters, the DDR3 SDRAM device supports  $tnPARAM [nCK] = RU\{ tPARAM [ns] / tCK(avg) [ns] \}$ , which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support  $tnRP = RU\{ tRP / tCK(avg) \}$ , which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support  $tnRP = RU\{ tRP / tCK(avg) \} = 6$ , as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.
5. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where  $2 \leq m \leq 12$ . (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then  $tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps$  and  $tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps$ . Similarly, tLZ(DQ) for DDR3-800 derates to  $tLZ(DQ),min(derated) = 800 ps - 193 ps = - 993 ps$  and  $tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps$ . (Caution on the min/max usage!) Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where  $2 \leq n \leq 12$ , and tERR(mper),act,max is the maximum measured value of tERR(nper) where  $2 \leq n \leq 12$ .
6. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then  $tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 \times tCK(avg),act + tJIT(per),act,min = 0.9 \times 2500 ps - 72 ps = + 2178 ps$ . Similarly,  $tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 \times tCK(avg),act + tJIT(per),act,min = 0.38 \times 2500 ps - 72 ps = + 878 ps$ . (Caution on the min/max usage!)=  $0.38 \times 2500 ps - 72 ps = + 878 ps$ . (Caution on the min/max usage!)

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**18.2 Timing Parameter Notes**

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON see "Device Operation"
8. For definition of RTT turn-off time tAOF see "Device Operation".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0
11. The maximum read postamble is bound by tDQCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. Device Operation.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is valid for RON34
14. Single ended signal parameter.
15. tREFI depends on TOPER
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET, VREF(DC)=VREFCA(DC). See "Address/ Command Setup, Hold and Derating"
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS differential slew rate. Note for DQ and DM signals, VREF(DC)= VREFDQ(DC). For input only pins except RESET, VREF(DC)=VREFCA(DC). See "Data Setup, Hold and Slew Rate Derating"
18. Start of internal write transaction is defined as follows ;  
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL  
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL  
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQCK(max) on the right side. See "Device Operation"
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation".
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% /°C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \sim 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

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25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC)
29. tDQSL describes the instantaneous differential input low pulse width on DQS-DQS, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS-DQS, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
32. tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

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**REVISION HISTORY**

Revision	Release Date	Description of Change	Checked By (Full Name)
X1	July 26, 2012	Preliminary release	Brian Ouellette
A	August 2, 2012	Initial Release	Brian Ouellette
A2	January 23, 2013	Added DDR3-1600 PN's capacitance, IDD and timing tables, Removed SCI from Sanmina-SCI company name. Removed unsupported CAS PN's	
A3	June 20, 2013	Revised mechanical drawing to show dimension in mm and a nominal thickness with tolerance.	
A4	August 28, 2013	Revised IDD values for 4GB 2rank DIMMs based on 4Gb DRAM data and removed the "Estimated values" note	
A5	October 3, 2013	Removed 1 rank IDD tables. Revised 4Gbit 2rank IDD table based on Hynix A die. Added "Estimated values" 2Gbit 2rank IDD table. Remove 4GB PN's. remove 1git based IDD table	
A6	12-Dec-13	Revised the tRFC for 4Gb from 300ns to 260ns	Chanhee Park
B	July 20, 2017	Revise logo. Change company address	

**STATEMENT OF COMPLIANCE**

Viking Technology(tm), Sanmina Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.

All printed circuit boards (PCBs) have a flammability rating of UL94V-0.

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