FLASH DATA RETENTION

Application Note

Document #AN0011 – Viking Flash Data Retention | Rev. B

Purpose of this Document

This application note was prepared to help OEM system designers evaluate the performance of Viking solid state drive solutions by using the same benchmarking methodology that Viking performs in it's SSD test facility. The SSD performance stated in the Viking SSD datasheets can be achieved by following the same Viking approach to SSD benchmarking which has been outlined in this document.

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1 Introduction

Fab process technologies for NAND Flash continue to shrink towards 20nm and less, while memory capacity increase beyond 64Gbit for multi-bit flash devices.

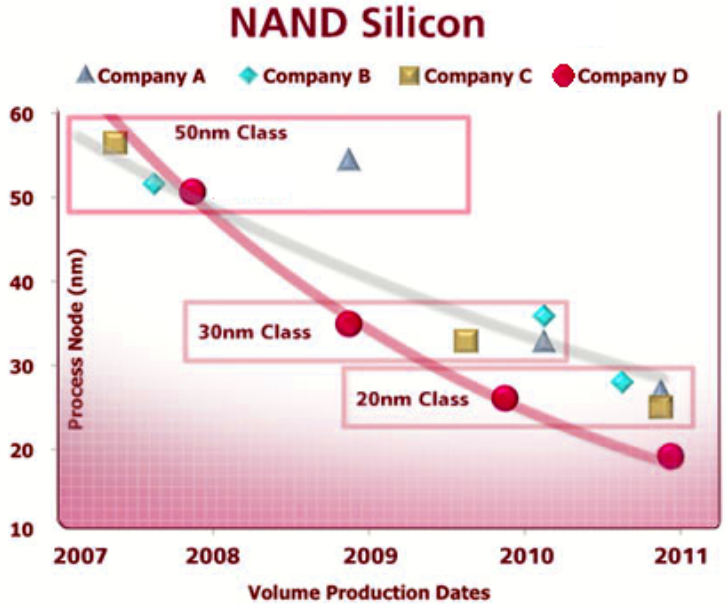

Figure 1-1: NAND Flash Fab Process Technology

However, this “scaling” of NAND flash MLC, (a.k.a. die shrinks) have the potential to reduce data retention and endurance of the flash due to certain effects on NAND flash floating gate transistors:

- Bit to Bit interaction
- Programming/Erase (P/E) oxide damage across the tunnel oxide channel
- Multiple failure modes (Detrapping and Stress Induced Leakage Current (SILC))

The JEDEC Data Retention specification for MLC Flash is:

- 10 years for P/E cycles <10% of the maximum of the P/E spec for the NAND
- 1 year for P/E cycles equaling the maximum for the P/E spec of the NAND flash

This document describes the flash failure mechanisms that affect Data Retention and JEDEC test methodology that determines the life of the flash based on program/erase cycles under elevated temperature cycling.

2 Mechanisms of Flash Failure that affects Data Retention

2.1 Data Retention Loss due to Detrapping

Flash cells store bits of data in the form of a charge on the floating gate of a floating gate transistor (cell) as shown in the following figures.

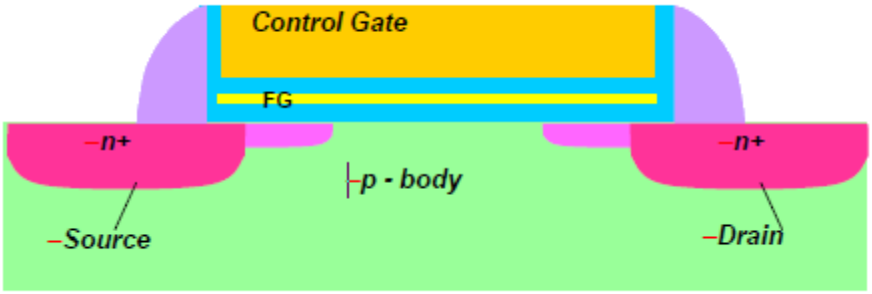

Figure 2-1: Floating Gate Transistor Construction

For NAND Flash, a Write (Program) operation is accomplished by a Fowler-Nordheim (FN) injection of electrons into the floating gate (FG). An erase is a reverse operation of the write that pushes the FN injection of electrons from FG into the substrate.

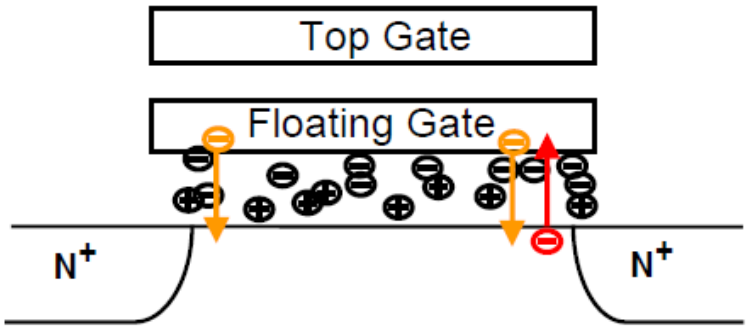

Figure 2-2: P/E of the Floating Gate Transistor

Repeated P/E operations cause damage to the tunnel oxide channel in the form of a "trapped charge" which affects the threshold voltage in the cell (in the range of 1.1 – 1.2eV). The data retention of the cell is lowered when the charge automatically "detraps" over time, causing the threshold voltage to shift and loose its data. This threshold shift is accelerated at a high number of P/E cycles and further accelerated at high temperatures as shown in the figure below.

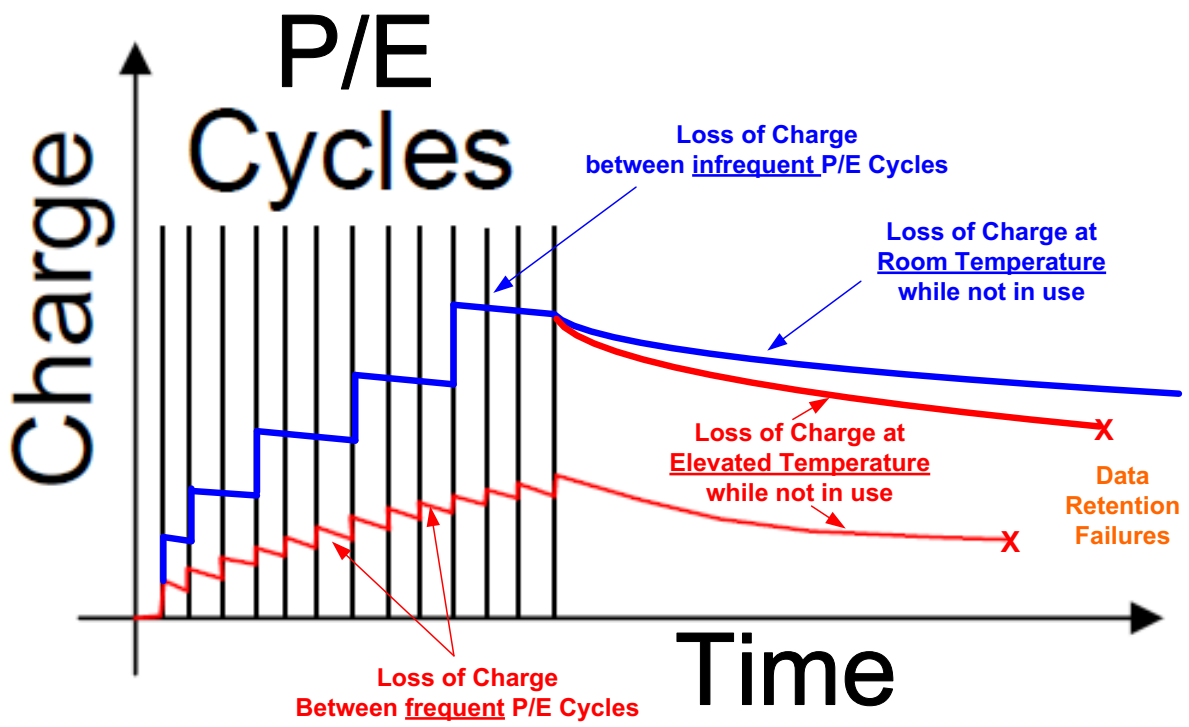

Figure 2-3: P/E Cycles and High Temperature both reduce Data Retention

The chart above shows the degradation rate of flash depend strongly on the cycling frequency because some cycling-induced damage mechanisms exhibit partial recovery in between cycles. Increasing the cycling rate may prevent that recovery from occurring and lead to early failures.

2.2 *Data Retention Loss due to Stress Induced Leakage Current (SILC)*

P/E cycling results in trapped charges in the oxide, which occasionally "line up" in pairs to strengthen and enhance trapped charge assisted tunneling. Data retention loss from SILC-related charge leakage (activation energy <0eV) has less temperature dependencies than charge detrapping.

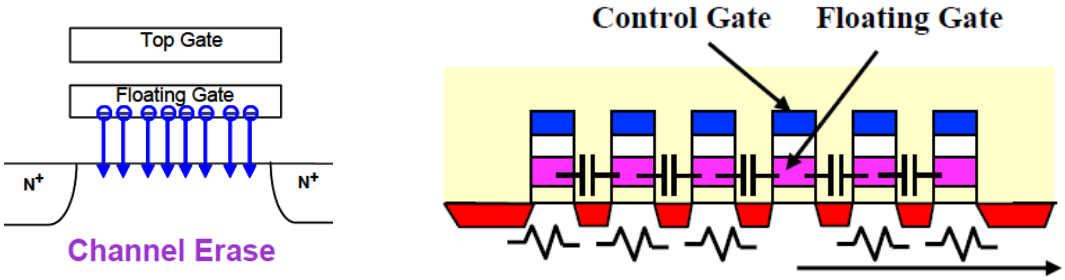

Figure 2-4: Stress Induced Leakage Current (SILC) Failure Mechanisms

3 JEDEC Test Method for Determining Data Retention

The failure mechanisms responsible for retention failures, are accelerated in different ways by temperature and other adjustable qualification parameters. For MLC NAND using floating-gate memories, as indicated in the previous section, failure may occur due to defects that allow charge to leak through the transfer dielectric (SILC) or by the detrapping of charge in the transfer dielectric. SILC can only be marginally accelerated or can even be decreased by high temperature, while Detrapping can be highly temperature-accelerated to induce data retention loss. Under user-mode application the product cycle count is spread over few years and the excess trapped charge may detrap between cycles, but if the product is run to maximum P/E cycle count in few days under qualification testing modes, excess trapped charge will build up, leading to early product failure during the endurance cycling itself or in the following data retention test. JEDEC document JEDEC-STD-JESD47G (Stress-Test-Driven Qualification of Integrated Circuits and JEDEC JESD22-A117 (Program/Erase Endurance and Data Retention Stress Test) cover this methodology in great detail.

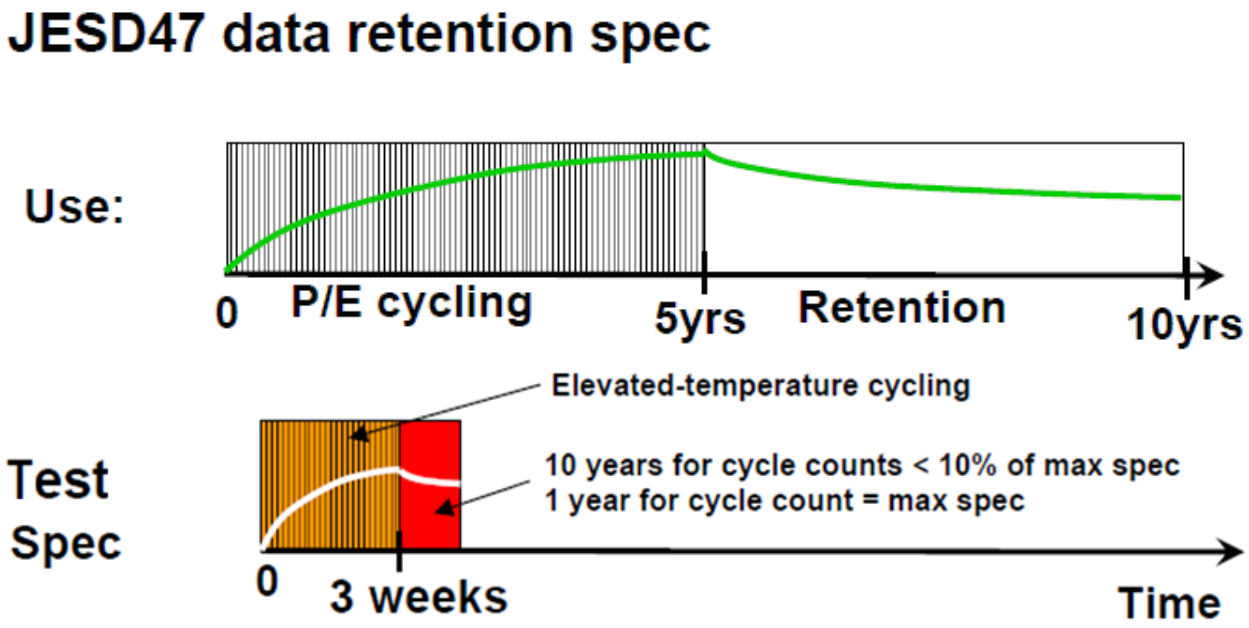

Figure 3-1: JEDEC Data Retention Test Spec

Notes:

1. The lined area indicates SSD programming/erase and solid area indicate no SSD activity

The JEDEC JESD47 test spec for flash memory is a Stress-Test-Driven Qualification of Integrated Circuits that specifies qualification requirements (test times, temperatures, sample sizes, etc.) to reflect the dominant failure mechanisms under realistic use conditions. JEDEC-STD-JESD 47 shows the # of hours of stress testing that would equate to # of years of actual use.

- Retention: Specifies a sliding retention scale (10 years for lower P/E cycle counts and 1 year for the maximum spec P/E cycle count)
  - Bake time/temperature chosen based on 1.1 eV activation energy for detrapping mechanism
  - 25°C temperature life test added after cycling to comprehend <0.0 eV mechanisms such as SILC

- Endurance: Specifies the fraction of high-density arrays that must be cycled
  - Block-level cycling with different cycle counts

The following test flow provides guidance on how to comprehend error correction and wear leveling in SSD's.

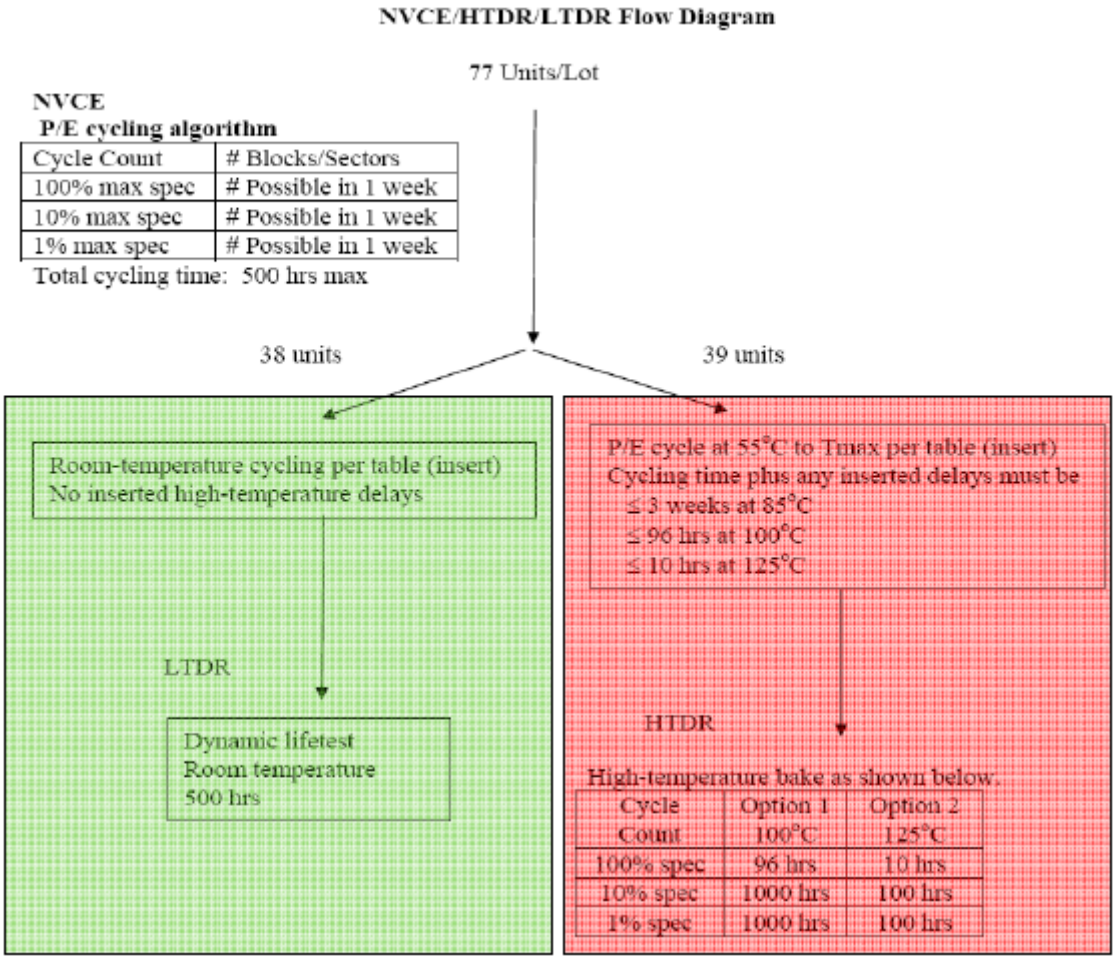

Figure 3-2: JEDEC Data Retention Test Flow

4 Summary

This paper shows that SSD data retention is inversely proportional to the rate or frequency of P/E cycles as well as the storage temperature of SSD. The JEDEC Data Retention specification for Flash stored at room temperature (less if at elevated temperatures) is:

- 10 years for P/E cycles <10% of the maximum of the P/E spec for the NAND
- 1 year for P/E cycles equaling the maximum for the P/E spec of the NAND flash

For SSD users, one way to lengthen the “shelf life” of an SSD near the end of it’s useful operating life, is to keep the P/E cycles less than the spec and store unused SSD’s at room temperature, or less.

5 Reference Documents

- JEDEC JEP122: Failure Mechanisms & Models for Semiconductor Devices.
  http://www.JEDEC.org
- JEDEC-STD-JESD47G: Stress-Test-Driven Qualification, Integrated Circuits
  http://www.JEDEC.org
- JEDEC JESD22-A117B: Endurance and Data Retention Stress Test
  http://www.JEDEC.org
- EIA JESD 94:2008: Application Specific Qualification Using Knowledge Based Test Methodology
- AEC document AECQ100-005 - Rev-C: Non-Volatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test
  http://www.aecouncil.com/AECDocuments.html

6 About Viking Technology

Viking Technology develops and delivers innovative high-technology products that optimize the value and performance of our customers' applications. Founded in 1989, Viking Technology has been providing Original Equipment Manufacturers (OEMs) with industry leading designs, engineering, product support and customer service for 20 years. For more information visit http://www.vikingtechnology.com.

7 Revision History

Related Products		Viking Element SSD Datasheets
Author		
Date		4-28-11
Document Number		AN0011
Date	**Edited by**	**Alteration to previous document revision**
9/14/17		Revise logo. Change company address

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