

MODULE CONFIGURATIONS

Viking Part Number	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR5WP647218EBP	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5WP647218EBS	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5WP647218EBW	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5WP647218EBY	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5WP647218EBZ	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5WP287218FBP	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5WP287218FBS	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5WP287218FBW	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5WP287218FBY	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5WP287218FBZ	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5WP567218GBP	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5WP567218GBS	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5WP567218GBW	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5WP567218GBY	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5WP567218GBZ	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5WP567218FEP	2GB	256Mx72	128M x 8 (18)	DDP FBGA	2	PC2-3200	CL3 (3-3-3)
VR5WP567218FES	2GB	256Mx72	128M x 8 (18)	DDP FBGA	2	PC2-4200	CL4 (4-4-4)
VR5WP567218FEW	2GB	256Mx72	128M x 8 (18)	DDP FBGA	2	PC2-5300	CL5 (5-5-5)
VR5WP567218FEY	2GB	256Mx72	128M x 8 (18)	DDP FBGA	2	PC2-6400	CL5 (5-5-5)
VR5WP567218FEZ	2GB	256Mx72	128M x 8 (18)	DDP FBGA	2	PC2-6400	CL6 (6-6-6)

Features

- Single 1.8V ± 0.1V Power Supply
- Burst Length (4, 8)
- Burst type (Sequential & Interleave)
- Auto & Self-Refresh.
- 8k/64ms Refresh Period.
- Differential CLK (#CLK) input.
- On-die termination (ODT)
- Off-chip driver (OCD) impedance calibration
- Serial Presence Detect with EEPROM.
- RoHS Compliant* (see last page)

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PIN CONFIGURATIONS

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VREF	123	VSS	32	VSS	154	DQ28	63	VDDQ	185	A3	92	DQ41	214	VSS
2	VSS	124	DQ4	33	DQ24	155	DQ29	64	A2	186	A1	93	VSS	215	DM5
3	DQ0	125	DQ5	34	DQ25	156	VSS	65	VDD	187	VDD	94	/DQS5	216	NC
4	DQ1	126	VSS	35	VSS	157	DM3	KEY				95	DQS5	217	VSS
5	VSS	127	DM0	36	/DQS3	158	NC					96	VSS	218	DQ46
6	/DQS0	128	NC	37	DQS3	159	VSS	66	VSS	188	CK0	97	DQ42	219	DQ47
7	DQS0	129	VSS	38	VSS	160	DQ30	67	VSS	189	/CK0	98	DQ43	220	VSS
8	VSS	130	DQ6	39	DQ26	161	DQ31	68	NC	190	VDD	99	VSS	221	DQ52
9	DQ2	131	DQ7	40	DQ27	162	VSS	69	VDD	191	A0	100	DQ48	222	DQ53
10	DQ3	132	VSS	41	VSS	163	CB4	70	A10/AP	192	BA1	101	DQ49	223	VSS
11	VSS	133	DQ12	42	CB0	164	CB5	71	BA0	193	VDD	102	VSS	224	CK2
12	DQ8	134	DQ13	43	CB1	165	VSS	72	VDD	194	/RAS	103	SA2	225	/CK2
13	DQ9	135	VSS	44	VSS	166	DM8	73	/WE	195	VDDQ	104	NC	226	VSS
14	VSS	136	DM1	45	/DQS8	167	NC	74	VDDQ	196	/S0	105	VSS	227	DM6
15	/DQS1	137	NC	46	DQS8	168	VSS	75	/CAS	197	VDDQ	106	/DQS6	228	NC
16	DQS1	138	VSS	47	VSS	169	CB6	76	VDDQ	198	ODT0	107	DQS6	229	VSS
17	VSS	139	CK1	48	CB2	170	CB7	77	*/S1	199	A13	108	VSS	230	DQ54
18	*/RESET	140	/CK1	49	CB3	171	VSS	78	**ODT1	200	VDD	109	DQ50	231	DQ55
19	NC	141	VSS	50	VSS	172	NC	79	VDDQ	201	NC	110	DQ51	232	VSS
20	VSS	142	DQ14	51	NC	173	VDDQ	80	NC	202	VSS	111	VSS	233	DQ60
21	DQ10	143	DQ15	52	VDDQ	174	**CKE1	81	VSS	203	DQ36	112	DQ56	234	DQ61
22	DQ11	144	VSS	53	CKE0	175	VDD	82	DQ32	204	DQ37	113	DQ57	235	VSS
23	VSS	145	DQ20	54	VDD	176	*A15	83	DQ33	205	VSS	114	VSS	236	DM7
24	DQ16	146	DQ21	55	†BA2	177	*A14	84	VSS	206	DM4	115	/DQS7	237	NC
25	DQ17	147	VSS	56	NC	178	VDDQ	85	/DQS4	207	NC	116	DQS7	238	VSS
26	VSS	148	DM2	57	VDDQ	179	A12	86	DQS4	208	VSS	117	VSS	239	DQ62
27	/DQS2	149	NC	58	A11	180	A9	87	VSS	209	DQ38	118	DQ58	240	DQ63
28	DQS2	150	VSS	59	A7	181	VDD	88	DQ34	210	DQ39	119	DQ59	241	VSS
29	VSS	151	DQ22	60	VDD	182	A8	89	DQ35	211	VSS	120	VSS	242	SDA
30	DQ18	152	DQ23	61	A5	183	A6	90	VSS	212	DQ44	121	SA0	243	SCL
31	DQ19	153	VSS	62	A4	184	VDDQ	91	DQ40	213	DQ45	122	SA1	244	VDDSPD

*Pins are not used in this module
 ** Pins are used for 2 rank modules
 † Pin used for 1Gbit devices (7218F)

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PIN FUNCTION DESCRIPTION

SYMBOL	TYPE	POLARITY	DESCRIPTION
CK0 ~ CK2 /CK0 ~ /CK2	IN	Positive Edge Negative Edge	Clock: CK and /CK are differential clock inputs. All addresses and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output data (DQs, DQS and /DQS) is referenced to the crossings of CK and /CK.
CKE0, CKE1	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
/S0 ~ /S3	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both S[0:3] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state.
ODT0, ODT1	IN	Active High	On-Die Termination control signals
/RAS, /CAS, /WE	IN	Active Low	CAS, WE When sampled at the positive rising edge of the clock, /CAS, /RAS, and /WE define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL18 inputs
VDDQ	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA [2:0]	IN	-	Selects which SDRAM bank of four or eight is activated.
A [An:0]	IN	-	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input/Output pins
DM [8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
VDD, VSS	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
DQS [17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
/DQS [17:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA [2:0]	IN	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.

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PIN FUNCTION DESCRIPTION

SYMBOL	TYPE	POLARITY	DESCRIPTION
SDA	I/O	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pullup.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDDSPD on the system planar to act as a pullup.
VDDSPD	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector, which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operations.

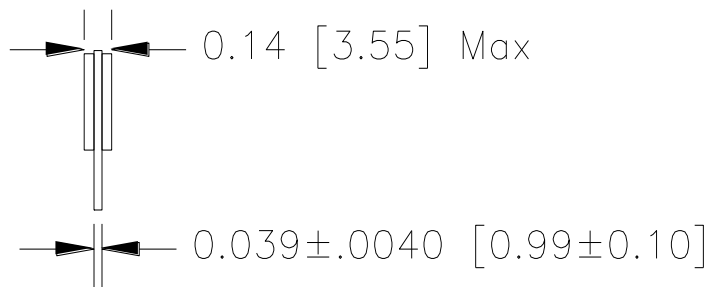
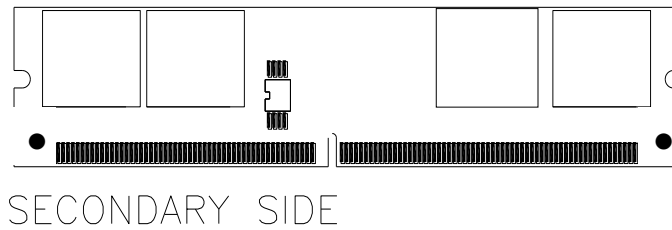
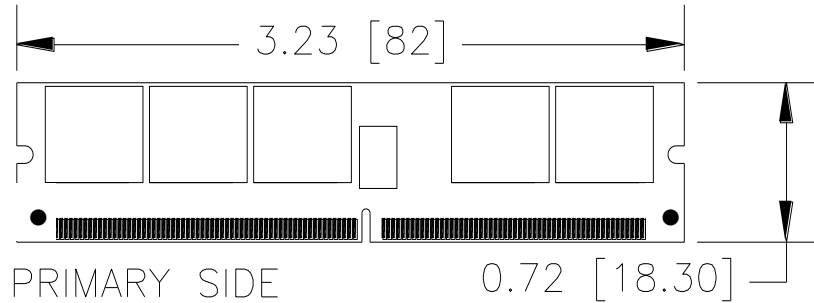
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MECHANICAL OUTLINE

Dimensions are in inches. (Tolerance is +/- 0.005, unless otherwise stated.)

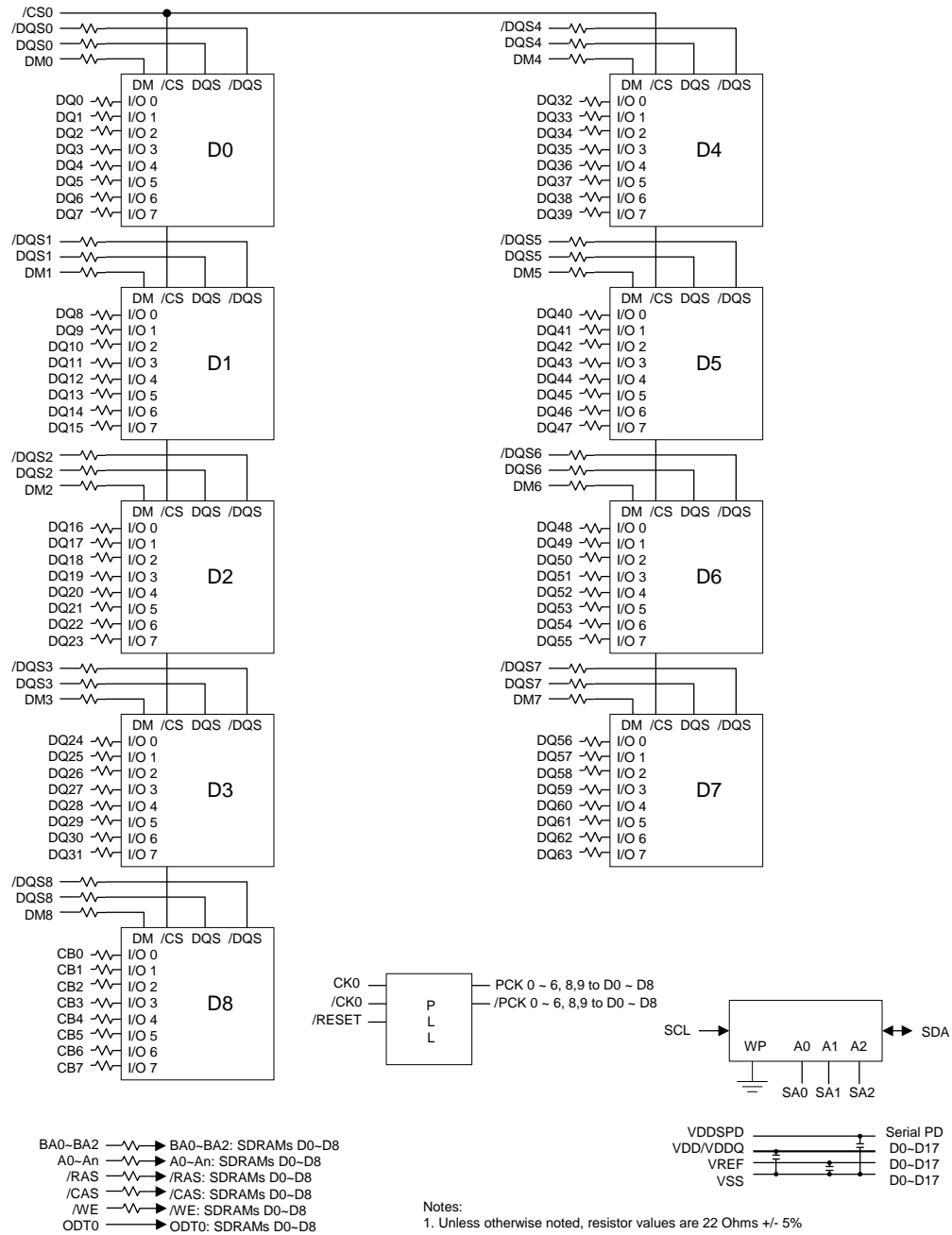


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FUNCTIONAL BLOCK DIAGRAM (Single Rank)

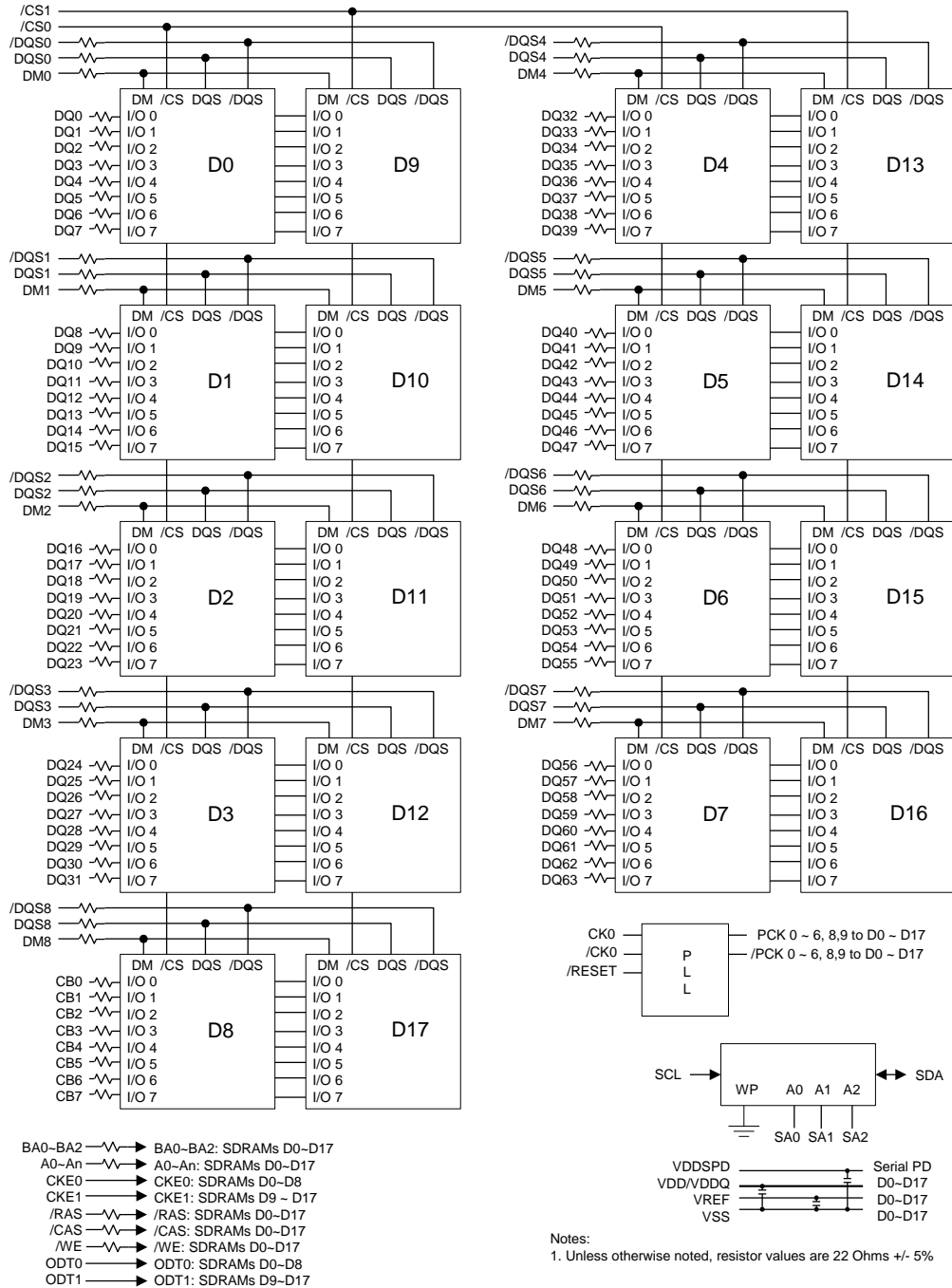


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FUNCTIONAL BLOCK DIAGRAM (Dual Rank)



ABSOLUTE MAXIMUM RATINGS

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Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND	Vin, Vout	-0.5 ~ 2.3	V
Voltage on VDD supply relative to GND	VDD	-1.0 ~ 2.3	V
Voltage on VDDQ supply relative to GND	VDDQ	-0.5 ~ 2.3	V
Storage temperature	TSTG	-55 ~ +100	°C

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_1.8)

Recommended operating conditions (Voltages referenced to GND, Tcase = 0 to 85°C)

Parameter	Symbol	Min.	Max.	Unit	Notes	
Case Temperature	Tcase	0	85	°C		
Supply voltage	VDD	1.7	1.9	V		
Supply voltage for DQ, DQS	VDDQ	1.7	1.9	V		
Input reference voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	1, 2	
EEPROM Supply Voltage	VDDSPD	1.7	3.6	V		
Input high voltage	VIH	VREF + 0.125	VDDQ + 0.3	V		
Input low voltage	VIL	-0.3	VREF - 0.125	V		
Input leakage current	Single Rank	IIL	-45	45	µA	3
Output leakage current	Single Rank	IOL	-5	5	µA	4
Input leakage current	Dual Rank	IIL	-90	90	µA	3
Output leakage current	Dual Rank	IOL	-10	10	µA	4

- Note:**
1. Peak to peak AC noise on VREF may not exceed +/- 2% VREF (DC). VREF is also expected to track noise variation in VDD.
 2. For any pin under test input of $0V \leq V_{IN} \leq V_{DDQ} + 0.3V$.
 3. Any input $0V \leq V_{IN} \leq V_{DD}$; all other pins not under test = 0V.
 4. $0V \leq V_{OUT} \leq V_{DDQ}$; DQ and ODT disabled

CAPACITANCE (VDD = 1.8V, TA = 25°C)

Parameter	Symbol	Min		Max		Unit	
		Single Rank	Dual Rank	Single Rank	Dual Rank		
Input capacitance (A0 ~ An, BA0 ~ BA1)	CIN1	14	23	23	41	pF	
Input capacitance (/RAS, /CAS, /WE)	CIN2	14	23	23	41	pF	
Input capacitance (CKE0 ~ *CKE1)	CIN3	14	23	23	41	pF	
Input capacitance (/S0)	CIN4	14		23		pF	
Input capacitance (CK0, /CK0 ~ CK2, /CK2)	CIN5a	8	11	11	17	pF	
Input capacitance (DQS0 ~ DQS7, /DQS0 ~ /DQS7), (DM0 ~ DM7)	400MHz, 533MHz	CIN6a	7.5	10	9	13	pF
	667MHz	CIN6c	7.5	10	8.5	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	400MHz, 533MHz	COUta	7.5	10	9	13	pF
	667MHz	COUtc	7.5	10	8.5	12	pF

*Used in dual module only

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DC CHARACTERISTICS DEFINITIONS (Recommended operating conditions unless otherwise noted, Tcase = 0 to 85 °C)

Note:

Parameter	Symbol	Test Condition	Unit	Note	
Operating one bank active-precharge current	IDD0	tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2	
Operating one bank active-read-precharge current	IDD1	IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2	
Precharge power-down current	IDD2P	All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3	
Precharge quiet standby current	IDD2Q	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3	
Precharge standby current	IDD2N	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3	
Active power-down current	IDD3P-F	All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MR(12) = 0	mA	1, 3
	IDD3P-S		Slow PDN Exit MR(12) = 1		
Active standby current	IDD3N	All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3	
Operating burst read current	IDD4R	All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2	
Operating burst write current	IDD4W	All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2	
Auto refresh current	IDD5	tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3	
Self refresh current	IDD6	CK and /CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	mA	1, 3	
Operating bank interleave read current	IDD7	All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R	mA	1, 2	

1. Calculated values are from component data. ODT disabled. IDD1 and IDD4R are defined with the outputs disabled. Currents are for DDR2 SDRAM components only.
2. Inactive ranks are in IDD2P Precharge Power-Down Standby Current mode.
3. All ranks are in the same IDD current mode.

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DC CHARACTERISTICS CURRENTS SINGLE RANK 512Mbit

Symbol	VR5WP647218EBP PC2-3200 CL3 (3-3-3)	VR5WP647218EBS PC2-4200 CL4 (4-4-4)	VR5WP647218EBW PC2-5300 CL5 (5-5-5)	VR5WP647218EBY/Z PC2-6400 CL5/CL6	Unit
IDD0	720	720	765	765	mA
IDD1	855	855	900	855	mA
IDD2P	72	72	72	72	mA
IDD2Q	270	270	315	315	mA
IDD2N	315	315	360	360	mA
IDD3P-F	270	270	270	270	mA
IDD3P-S	108	108	108	108	mA
IDD3N	450	450	495	540	mA
IDD4R	990	1125	1305	1305	mA
IDD4W	990	1080	1260	1035	mA
IDD5	1260	1260	1350	1035	mA
IDD6	72	72	72	72	mA
IDD7	1980	1980	1980	1935	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 1Gbit

Symbol	VR5WP287218FBP PC2-3200 CL3 (3-3-3)	VR5WP287218FBS PC2-4200 CL4 (4-4-4)	VR5WP287218FBW PC2-5300 CL5 (5-5-5)	VR5WP647218EBY/Z PC2-6400 CL5/CL6	Unit
IDD0	765	765	810	900	mA
IDD1	855	855	900	990	mA
IDD2P	135	135	135	63	mA
IDD2Q	360	405	405	585	mA
IDD2N	360	405	405	630	mA
IDD3P-F	315	315	360	450	mA
IDD3P-S	162	162	162	162	mA
IDD3N	495	540	540	675	mA
IDD4R	1035	1170	1395	1710	mA
IDD4W	1035	1170	1395	1665	mA
IDD5	1890	1935	1980	1400	mA
IDD6	135	135	135	63	mA
IDD7	2340	2520	2700	3015	mA

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DC CHARACTERISTICS CURRENTS DUAL RANK 1Gbit

Symbol	VR5WP567218FEP PC2-3200 CL3 (3-3-3)	VR5WP567218FES PC2-4200 CL4 (4-4-4)	VR5WP647218EBY/Z PC2-6400 CL5/CL6	Unit
IDD0	900	900	945	mA
IDD1	990	990	1035	mA
IDD2P	270	270	270	mA
IDD2Q	720	810	810	mA
IDD2N	720	810	810	mA
IDD3P-F	360	360	720	mA
IDD3P-S	324	324	324	mA
IDD3N	990	1080	1080	mA
IDD4R	1170	1305	1530	mA
IDD4W	1170	1305	1530	mA
IDD5	3780	3870	3960	mA
IDD6	270	270	270	mA
IDD7	2475	2655	2835	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 2Gbit

Symbol	VR5WP567218GBP PC2-3200 CL3 (3-3-3)	VR5WP567218GBS PC2-4200 CL4 (4-4-4)	VR5WP567218GBW PC2-5300 CL5 (5-5-5)	VR5WP647218EBY/Z PC2-6400 CL5/CL6	Unit
IDD0	765	765	810	855	mA
IDD1	855	855	900	945	mA
IDD2P	108	108	108	108	mA
IDD2Q	360	360	405	450	mA
IDD2N	405	405	450	495	mA
IDD3P-F	315	315	315	315	mA
IDD3P-S	162	162	162	162	mA
IDD3N	540	540	630	720	mA
IDD4R	1485	1485	1665	1980	mA
IDD4W	1620	1620	1800	2160	mA
IDD5	1890	1890	1980	2070	mA
IDD6	135	135	135	135	mA
IDD7	2295	2295	2520	2745	mA

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AC INPUT TEST CONDITIONS

Parameter	Symbol	Value	Unit	Notes
Input reference voltage	VREF	0.50 * VDDQ	V	
Input signal maximum peak to peak swing	VSWING _(MAX)	1.0	V	
Input signal maximum slew rate	SLEW	1.0	V/ns	1, 2

Notes:

1. The Input signal minimum slew rate is to be maintain over the range from VIL(DC) max to VIL(AC) min for raising edges and the range from VIH(DC) min to VIL(AC) max for falling edges.
2. AC timings are reference with input waveforms switching from VIL(AC) to VIH(AC) on the positive transition and VIH(AC) to VIL(AC) on the negative transitions.

AC OPERATING CONDITIONS (VDD = 1.8V ± 0.1V, TOPR = 0 to 85 °C)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Input Differential Voltage	VID(ac)	0.5	VDDQ +0.6	V	1
Input Crossing Point Voltage	VIX(ac)	0.5*VDDQ -0.175	0.5*VDDQ +0.175	V	2

Notes:

1. VID (AC) specifies the input differential voltage $I_{Vtr} - V_{cp}$ required for switching, where V_{tr} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{cp} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to VIH (AC) – VIL (AC).
2. The typical value of Vix (AC) is expected to be about 0.5 x VDDQ of the transmitting devices and Vix (AC) is expected to track variations in VDDQ.

OCD Default Characteristics

Description	Min	Nom	Max	Unit	Notes
Output Impedance	12.6	18	23.4	Ohms	1, 2
Pull-Up and Pull-Down mismatch	0	-	4	Ohms	1, 2, 3
Output slew rate	1.5	-	4.5	V/ns	1, 4, 5

Notes:

1. Absolute specifications: 0°C ≤ Tcase ≤ 85°C; VDD = 1.8V +/- 0.1V, VDDQ = 1.8V +/- 0.1V.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

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AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Symbol	Parameter	PC2-3200		PC2-4200		PC2-5300		PC2-6400		Units
		min	max	min	max	min	max	min	max	
tAC	DQ output access time from CK/CK	-600	+600	-500	+500	-450	+450	-400	400	ps
tDQSCK	DQS output access time from CK/CK	-500	+500	-450	+450	-400	+400	-350	350	ps
tCH	CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tHP	CK half period	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ps
tCK	Clock cycle time, CL=x	5000	8000	3750	8000	3000	8000	2500	8000	ps
tDH(base)	DQ and DM input hold time	275	x	225	x	175	x	125	x	ps
tDS(base)	DQ and DM input setup time	150	x	100	x	100	x	50	x	ps
tIPW	Control & Address input pulse width for each input	0.6	x	0.6	x	0.6	x	0.6	x	tCK
tDIPW	DQ and DM input pulse width for each input	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tHZ	Data-out high-impedance time from CK/CK	x	tAC max	x	tAC max	x	tAC max	x	tAC max	ps
tLZ(DQS)	DQS low-impedance time from CK/CK	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
tLZ(DQ)	DQ low-impedance time from CK/CK	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	ps
tDQSQ	DQS-DQ skew for DQS and associated DQ signals	x	350	x	300	x	240	x	200	ps
tQHS	DQ hold skew factor	x	450	x	400	x	340	x	300	ps
tQH	DQ/DQS output hold time from DQS	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps
tDQSS	First DQS latching transition to associated clock edge	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK
tDQSH	DQS input high pulse width	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tDQSL	DQS input low pulse width	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tDSS	DQS falling edge to CK setup time	0.2	x	0.2	x	0.2	x	0.2	x	tCK
tDSH	DQS falling edge hold time from CK	0.2	x	0.2	x	0.2	x	0.2	x	tCK
tMRD	Mode register set command cycle time	2	x	2	x	2	x	2	x	tCK
tWPST	Write postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tWPRE	Write preamble	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tIH(base)	Address and control input hold time	475	x	375	x	275	x	250	x	ps
tIS(base)	Address and control input setup time	350	x	250	x	200	x	175	x	ps
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tRRD	Active to active command period for 1kb page size products	7.5	x	7.5	x	7.5	x	7.5	x	ns
tRRD	Active to active command period for 2kb page size products	10	x	10	x	10	x	10	x	ns
tFAW	Four Bank Activate period for 1kb page size products	37.5		37.5		37.5		35		ns
tFAW	Four Bank Activate period for 2kb page size products	50		50		50		45		ns
tCCD	CAS to CAS command delay	2		2		2		2	x	tCK
tWR	Write recovery time	15	x	15	x	15	x	15	x	ns

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AC CHARACTERISTICS

Symbol	Parameter		PC2-3200		PC2-4200		PC2-5300		PC2-6400		Units	
			min	max	min	max	min	max	min	max		
tRC	Active to Active/Auto-Refresh command period		CL = 3	55	-	-	-	-	-	-	ns	
			CL = 4	-	-	60	-	-	-	-		
			CL = 5	-	-	-	60	-	57.5	-		
			CL = 6	-	-	-	-	-	60	-		
tRFC	Auto-Refresh to Active/Auto-Refresh command period		256Mb, 512Mb	105	70000	105	70000	105	70000	105	70000	ns
			1Gb	127.5	-	127.5	-	127.5	-	127.5	-	
			2Gb	195	-	195	-	195	-	195	-	
tRCD	Active to Read or Write (with and without Auto-Precharge) delay		CL = 3	15	-	-	-	-	-	-	ns	
			CL = 4	-	-	15	-	-	-	-		
			CL = 5	-	-	-	-	15	-	12.5		-
			CL = 6	-	-	-	-	-	-	15		-
tRP	Precharge command period		CL = 3	15	-	-	-	-	-	-	ns	
			CL = 4	-	-	15	-	-	-	-		
			CL = 5	-	-	-	-	15	-	12.5		-
			CL = 6	-	-	-	-	-	-	15		-
tRAS	Active to Precharge command		CL = 3	40	70000	-	70000	-	70000	-	70000	ns
			CL = 4	-	-	45	-	-	-	-		
			CL = 5	-	-	-	-	45	-	45	-	
			CL = 6	-	-	-	-	-	-	45	-	
tDAL	Auto precharge write recovery + precharge time		WR+tRP	x	WR+tRP	x	WR+tRP	x	WR+tRP	x	tCK	
tWTR	Internal write to read command delay		10	x	7.5	x	7.5	x	7.5		ns	
tRTP	Internal read to precharge command delay		7.5		7.5		7.5		7.5		ns	
tXSNR	Exit self refresh to a non-read command		tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns	
tXSRD	Exit self refresh to a read command		200		200		200		200	x	tCK	
tXP	Exit precharge power down to any non-read command		2	x	2	x	2	x	2	x	tCK	
tXARD	Exit active power down to read command		2	x	2	x	2	x	2	x	tCK	
tXARDS	Exit active power down to read command (slow exit, lower power)		6 - AL		6 - AL		7 - AL		8 - AL		tCK	
t ^{CKE}	CKE minimum pulse width (high and low pulse width)		3		3		3		3		tCK	
t ^{AOND}	ODT turn-on delay		2	2	2	2	2	2	2	2	tCK	
t ^{AON}	ODT turn-on		tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+0.7	ns	
t ^{AONPD}	ODT turn-on(Power-Down mode)		tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns	
t ^{AOFD}	ODT turn-off delay		2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK	
t ^{AOF}	ODT turn-off		tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	
t ^{AOFPD}	ODT turn-off (Power-Down mode)		tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
tANPD	ODT to power down entry latency		3		3		3		3		tCK	
tAXPD	ODT power down exit latency		8		8		8		8		tCK	
tOIT	OCD drive mode output delay		0	12	0	12	0	12	0	12	ns	
tDelay	Minimum time clocks remain ON after CKE asynchronously drops LOW		tIS+tCK+tIH		tIS+tCK+tIH		tIS+tCK+tIH		tIS+tCK+tIH		ns	

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REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
X1	January 11, 2008	Preliminary release	Brian Ouellette
X2	January 14, 2008	Remove register input from features	Brian Ouellette
A	January 31, 2008	Initial release	Brian Ouellette & John Le
B	February 19, 2009	Removed stacked BGA, add 2Gb mono	Brian Ouellette
C	October 22, 2009	Add DDP configurations	Brian Ouellette
D	May 3, 2010	Correct MO height	Brian Ouellette
D1	July 30, 2012	Add new logo and company name	
E	January 14, 2015	Update PCB drawing per PCB 1201 (A001730)	
F	April 20, 2015	Update PCB drawing with mounting holes	
G	March 20, 2017	Revise logo. Change company address. Add CL6 PN's	

STATEMENT OF COMPLIANCE

Viking , Sanmina-SCI Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.

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