DDR2 PC2-xx00
ECC REGISTERED SODIMM
VR5DRxx7218xxx

Module Configuration

Viking Part Number	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR5DR647218EBP	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5DR647218EBS	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5DR647218EBW	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5DR647218EBZ	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5DR647218EBY	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5DR287218EBP	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5DR287218EBS	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5DR287218EBW	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5DR287218EBZ	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-6400	CL6 (6-6-6)
VR5DR287218EBY	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5DR287218FBP	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5DR287218FBS	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5DR287218FBW	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5DR287218FBZ	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5DR287218FBY	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5DR567218FBP	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5DR567218FBS	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5DR567218FBW	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5DR567218FBZ	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-6400	CL6 (6-6-6)
VR5DR567218FBY	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5DR127218GBP	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5DR127218GBS	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5DR127218GBW	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5DR127218GBZ	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-6400	CL6 (6-6-6)
VR5DR127218GBY	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-6400	CL5 (5-5-5)

Features

- 200 pin Registered SO-DIMM JEDEC pin out
- Single 1.8V ± 0.1V Power Supply
- Burst Length (4, 8)
- Burst type (Sequential & Interleave)
- Auto & Self-Refresh.
- 7.8 µs Average Refresh Period.
- Differential CLK (#CLK) input.
- On-die termination (ODT)
- Off-chip driver (OCD) impedance adjustment
- Serial Presence Detect with EEPROM.
- RoHS Compliant* (see last page)

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Pb-FREE

PIN CONFIGURATIONS

Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK
1	VREF	2	VSS	51	DQ18	52	VSS	101	VDD	102	A6	151	VSS	152	VSS
3	DQ0	4	DQ4	53	DQ19	54	DQ28	103	A5	104	A4	153	#DQS5	154	DM5
5	VSS	6	DQ5	55	VSS	56	DQ29	105	A3	106	VDD	155	DQS5	156	VSS
7	DQ1	8	VSS	57	DQ24	58	VSS	107	A2	108	A1	157	VSS	158	DQ46
9	#DQS0	10	DM0	59	DQ25	60	DM3	109	VDD	110	A0	159	DQ42	160	DQ47
11	DQS0	12	VSS	61	VSS	62	VSS	111	A10/AP	112	BA1	161	DQ43	162	VSS
13	VSS	14	DQ6	63	#DQS3	64	DQ30	113	BA0	114	VDD	163	VSS	164	DQ52
15	DQ2	16	DQ7	65	DQS3	66	DQ31	115	#RAS	116	#WE	165	DQ48	166	DQ53
17	DQ3	18	VSS	67	VSS	68	VSS	117	VDD	118	#S0	167	DQ49	168	VSS
19	VSS	20	DQ12	69	DQ26	70	CB4	119	#CAS	120	ODT0	169	VSS	170	DM6
21	DQ8	22	DQ13	71	DQ27	72	CB5	121	#S1*	122	A13	171	#DQS6	172	VSS
23	DQ9	24	VSS	73	VSS	74	VSS	123	VDD	124	VDD	173	DQS6	174	DQ54
25	VSS	26	DM1	75	CB0	76	DM8	125	ODT1*	126	CK0	175	VSS	176	DQ55
27	#DQS1	28	VSS	77	CB1	78	VSS	127	NC	128	#CK0	177	DQ50	178	VSS
29	DQS1	30	DQ14	79	VSS	80	CB6	129	DQ32	130	VSS	179	DQ51	180	DQ60
31	VSS	32	DQ15	81	#DQS8	82	CB7	131	VSS	132	DQ36	181	VSS	182	DQ61
33	DQ10	34	VSS	83	DQS8	84	VSS	133	DQ33	134	DQ37	183	DQ56	184	VSS
35	DQ11	36	DQ20	85	VSS	86	CB2	135	#DQS4	136	VSS	185	DQ57	186	DM7
37	VSS	38	DQ21	87	CKE0	88	CB3	137	DQS4	138	DM4	187	VSS	188	DQ62
39	DQ16	40	VSS	89	CKE1*	90	VSS	139	VSS	140	VSS	189	#DQS7	190	VSS
41	DQ17	42	#RESET	91	NC	92	BA2**	141	DQ34	142	DQ38	191	DQS7	192	DQ63
43	VSS	44	DM2	93	VDD	94	NC/A14†	143	DQ35	144	DQ39	193	DQ58	194	SDA
45	#DQS2	46	VSS	95	A12	96	A11	145	VSS	146	VSS	195	VSS	196	SCL
47	DQS2	48	DQ22	97	A9	98	VDD	147	DQ40	148	DQ44	197	DQ59	198	SA1
49	VSS	50	DQ23	99	A7	100	A8	149	DQ41	150	DQ45	199	VDDSPD	200	SA0

*Not used in single rank configuration
**Used these pin in the 1Gbit and up device
† Used for 2Gb SDRAM configurations.

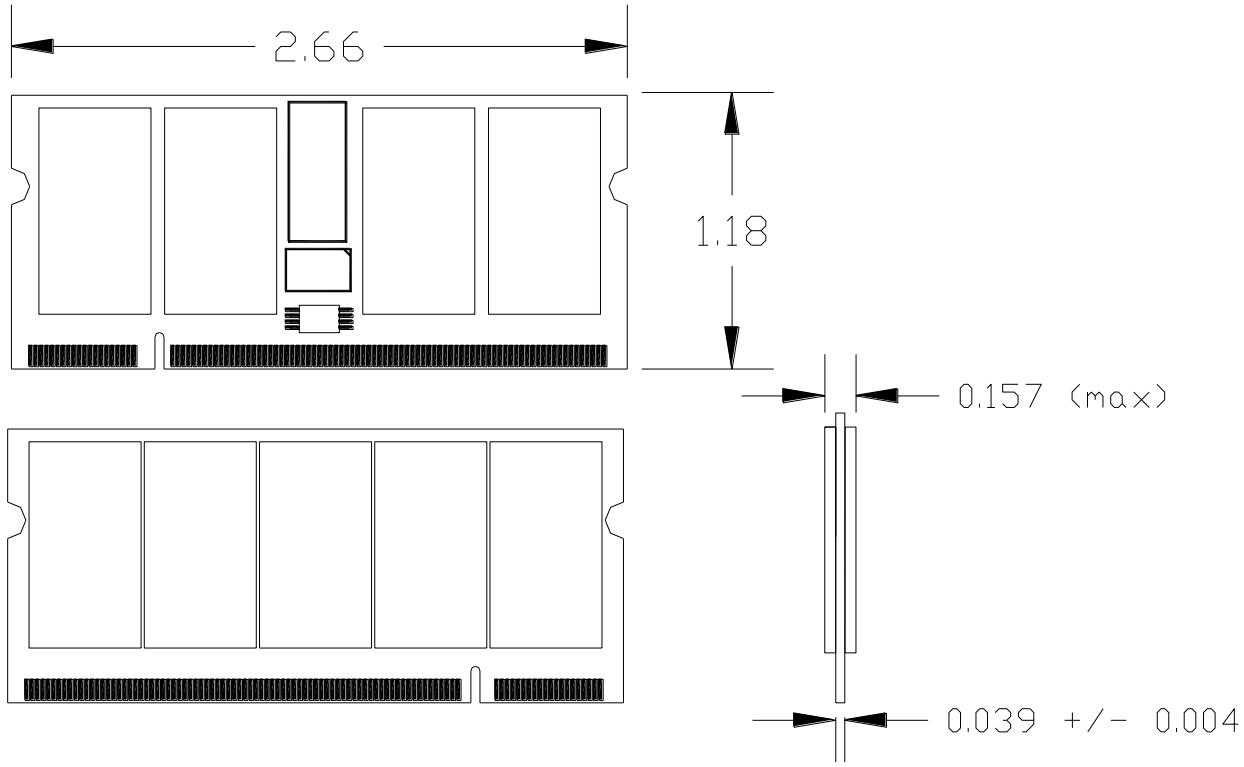
PIN FUNCTION DESCRIPTION

SYMBOL	TYPE	POLARITY	DESCRIPTION
CK0 #CK0	IN	Positive Edge Negative Edge	Clock: CK and #CK are differential clock inputs. All addresses and control input signals are sampled on the crossing of the positive edge of CK and negative edge of #CK. Output data (DQs, DQS and #DQS) is referenced to the crossings of CK and #CK.
CKE0 ~ CKE1	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
#S0 ~ #S1	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both S[0:1] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state.
ODT0 ~ ODT1	IN	Active High	On-Die Termination control signals
#RAS, #CAS, #WE	IN	Active Low	CAS, WE When sampled at the positive rising edge of the clock, /CAS, /RAS, and /WE define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL18 inputs
VDD, VDDQ	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA [2:0]	IN	-	Selects which SDRAM bank of four or eight is activated.
A [n:0]	IN	-	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1,BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input/Output pins
DM [8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
DQS [8:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
#DQS [8:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA [1:0]	IN	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pullup.
VDDSPD	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operations.

SYMBOL	TYPE	POLARITY	DESCRIPTION
/RESET	IN		The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)

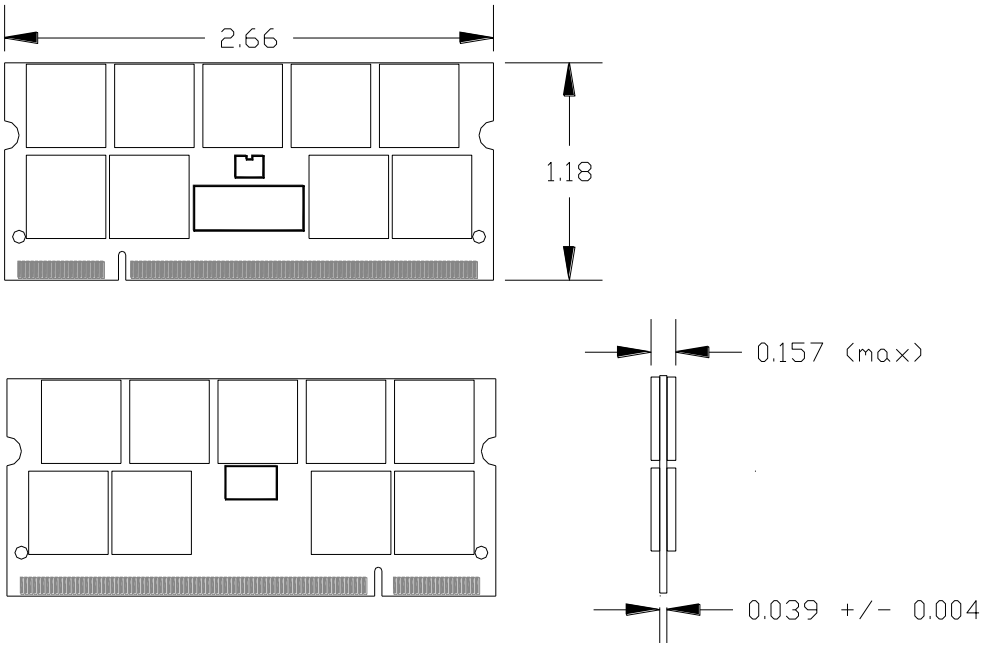
MECHANICAL OUTLINE (Single Rank)

Dimensions are inches. Tolerance is +/- 0.005, unless otherwise stated.

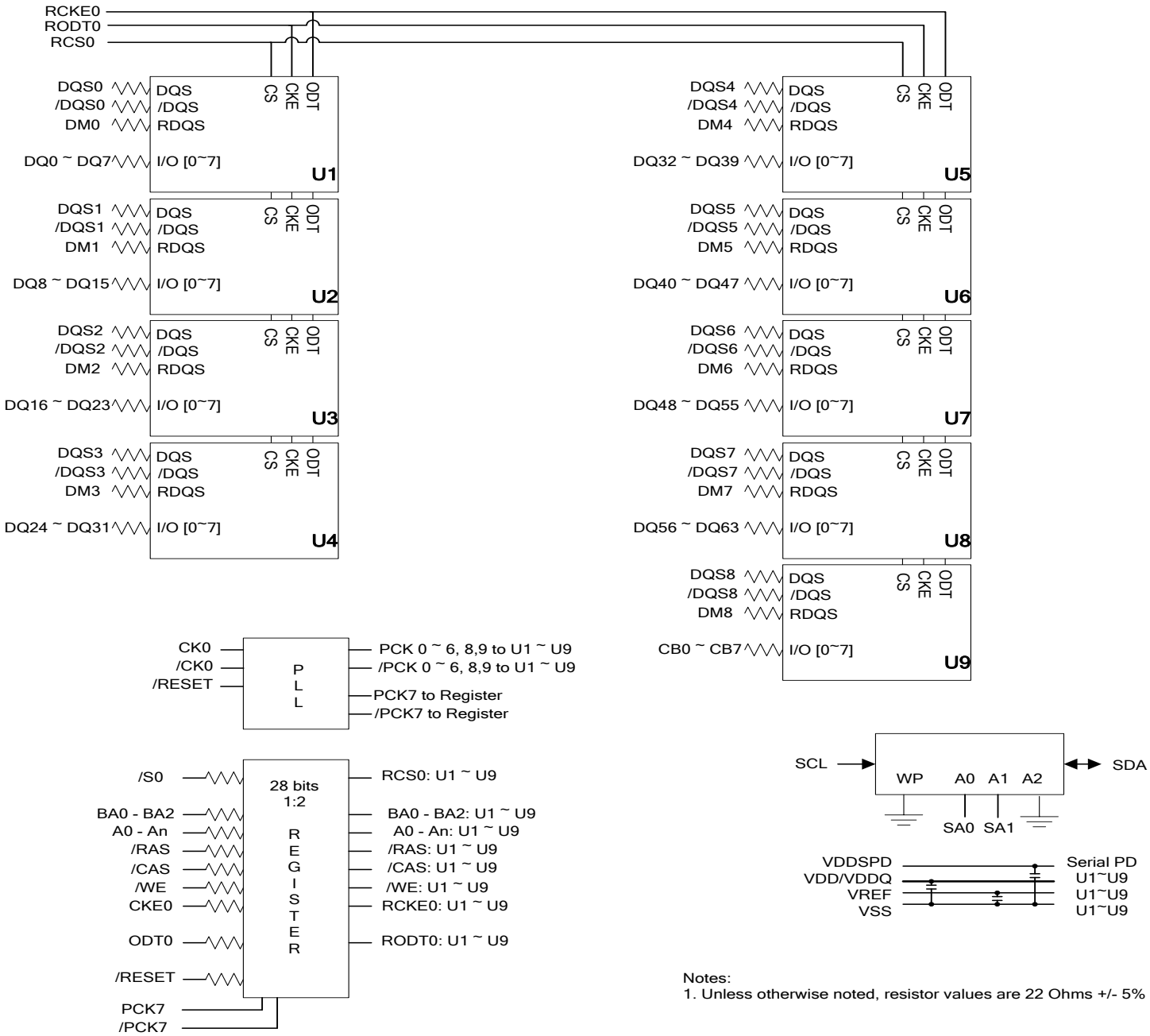


MECHANICAL OUTLINE (Dual Rank)

Dimensions are inches. Tolerance is +/- 0.005, unless otherwise stated.

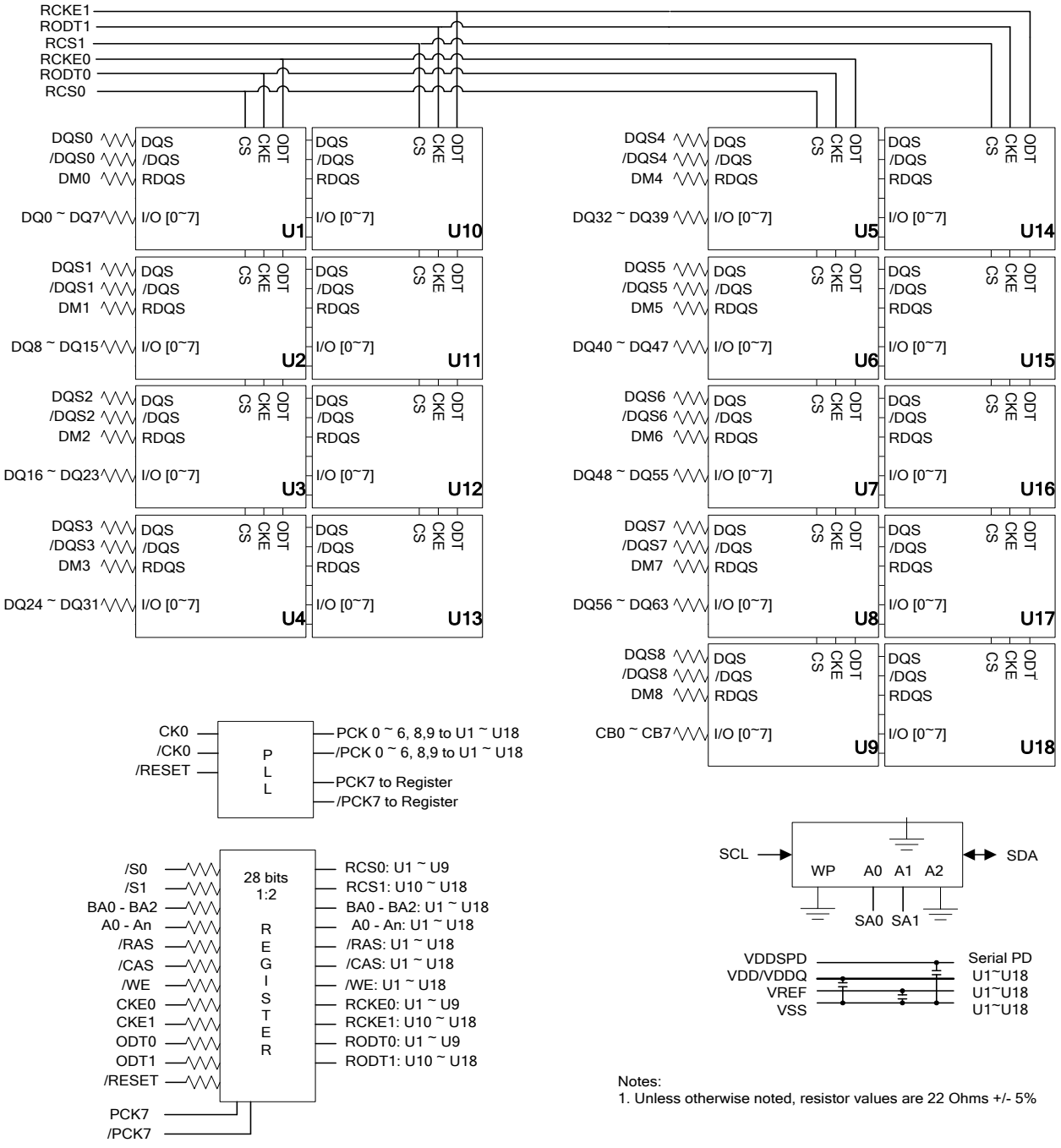


FUNCTIONAL BLOCK DIAGRAM (Single Rank)



Notes:
1. Unless otherwise noted, resistor values are 22 Ohms +/- 5%

FUNCTIONAL BLOCK DIAGRAM (Dual Rank)



Notes:
1. Unless otherwise noted, resistor values are 22 Ohms +/- 5%

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND	Vin, Vout	-0.5 ~ 2.3	V
Voltage on VDD supply relative to GND	VDD	-1.0 ~ 2.3	V
Voltage on VDDQ supply relative to GND	VDDQ	-0.5 ~ 2.3	V
Storage temperature	TSTG	-55 ~ +100	°C

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_1.8)

Recommended operating conditions (Voltages referenced to GND, Tcase = 0 to 85°C)

Parameter		Symbol	Min.	Max.	Unit	Notes
Case Temperature		Tcase	0	85	ºC	
Supply voltage		VDD	1.7	1.9	V	
Supply voltage for DQ, DQS		VDDQ	1.7	1.9	V	
Input reference voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	1, 2
EEPROM Supply Voltage		VDDSPD	1.7	3.6	V	
Input high voltage		VIH	VREF + 0.125	VDDQ + 0.3	V	
Input low voltage		VIL	-0.3	VREF - 0.125	V	
Input leakage current	Single Rank	IIL	-5	5	µA	3
Input leakage current	Dual Rank	IIL	-5	5	µA	3
Output leakage current	Single Rank	IOL	-5	5	µA	4
Output leakage current	Dual Rank	IOL	-10	10	µA	4

Note: 1. Peak to peak AC noise on VREF may not exceed +/- 2% VREF (DC). VREF is also expected to track noise variation in VDD.
2. For any pin under test input of 0 V ≤ VIN ≤ VDDQ +0.3 V.
3. Any input 0V≤Vin≤VDD; all other pins not under test = 0V.
4. 0V≤VOUT≤VDDQ; DQ and ODT disabled

CAPACITANCE (VDD = 1.8V, TA = 25ºC)

Parameter		Symbol	Min		Max		Unit
			Single Rank	Dual Rank	Single Rank	Dual Rank	
Input capacitance (A0 ~ An, BA0 ~ BA1)		CIN1	7.5		9		pF
Input capacitance (#RAS, #CAS, #WE)		CIN2	7.5		9		pF
Input capacitance (CKE0 ~ *CKE1, ODT0 ~ *ODT1)		CIN3	7.5		9		pF
Input capacitance (#S0 ~*#S1)		CIN4	7.5		9		pF
Input capacitance (CK0, #CK0)		CIN5a	7		8		pF
Input capacitance (DQS0 ~ DQS7, /DQS0 ~ /DQS7), (DM0 ~ DM7)	400MHz, 533MHz	CIN6a	7.5	10	9	13	pF
	667MHz, 800MHz	CIN6b	7.5	10	8.5	12.5	pF
Data input/output capacitance (DQ0 ~ DQ63, CB0 ~ CB7)	400MHz, 533MHz	CIN7a	7.5	10	9	13	pF
	667MHz, 800MHz	CIN7b	7.5	10	8.5	12.5	pF

*Used in dual rank module only

DC CHARACTERISTICS DEFINITIONS (Recommended operating conditions unless otherwise noted, Tcase = 0 to 85 °C)

Parameter	Symbol	Test Condition		Unit	Note
Operating one bank active-precharge current	IDD0	tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 2
Operating one bank active-read-precharge current	IDD1	IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	1, 2
Precharge power-down current	IDD2P	All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	1, 3
Precharge quiet standby current	IDD2Q	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	1, 3
Precharge standby current	IDD2N	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 3
Active power-down current	IDD3P-F	All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MR(12) = 0	mA	1, 3
	IDD3P-S		Slow PDN Exit MR(12) = 1		
Active standby current	IDD3N	All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 3
Operating burst read current	IDD4R	All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	1, 2
Operating burst write current	IDD4W	All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 2
Auto refresh current	IDD5	tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 3
Self refresh current	IDD6	CK and /CK at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		mA	1, 3
Operating bank interleave read current	IDD7	All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R		mA	1, 2

Note: 1. Calculated values are from component data. ODT disabled. IDD1, TDD4R are defined with the outputs disabled.
2. For dual rank modules the other rank is in IDD2P Precharge Power-Down Standby Current mode.
3. For dual rank modules both ranks are in the same IDD current mode.

DC CHARACTERISTICS CURRENTS SINGLE RANK 512Mbit

Symbol	VR5DR647218EBP PC2-3200 CL3 (3-3-3)	VR5DR647218EBS PC2-4200 CL4 (4-4-4)	VR5DR647218EBW PC2-5300 CL5 (5-5-5)	VR5DR647218EBY/Z PC2-6400 CL5 (5-5-5) / PC2-6400 CL6 (6-6-6)	Unit
IDD0	720	720	765	765	mA
IDD1	855	855	900	855	mA
IDD2P	72	72	72	72	mA
IDD2Q	270	270	315	315	mA
IDD2N	315	315	360	360	mA
IDD3P-F	270	270	270	270	mA
IDD3P-S	108	108	108	108	mA
IDD3N	450	450	495	540	mA
IDD4R	990	1125	1305	1260	mA
IDD4W	990	1080	1260	990	mA
IDD5	1260	1260	1350	990	mA
IDD6	72	72	72	72	mA
IDD7	1980	1980	1980	1890	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 512Mbit

Symbol	VR5DR287218EBP PC2-3200 CL3 (3-3-3)	VR5DR287218EBS PC2-4200 CL4 (4-4-4)	VR5DR287218EBW PC2-5300 CL5 (5-5-5)	VR5DR287218EBY/Z PC2-6400 CL5 (5-5-5) / PC2-6400 CL6 (6-6-6)	Unit
IDD0	927	1080	1125	837	mA
IDD1	1062	1215	1260	927	mA
IDD2P	144	180	180	144	mA
IDD2Q	360	450	450	630	mA
IDD2N	450	540	630	720	mA
IDD3P-F	630	720	720	540	mA
IDD3P-S	360	450	450	216	mA
IDD3N	1080	1170	1260	1080	mA
IDD4R	1422	1800	2160	1332	mA
IDD4W	1422	1800	2070	1062	mA
IDD5	4140	4500	4860	1980	mA
IDD6	108	108	108	144	mA
IDD7	2772	2970	2970	1962	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 1Gbit

Symbol	VR5DR287218FBP PC2-3200 CL3 (3-3-3)	VR5DR287218FBS PC2-4200 CL4 (4-4-4)	VR5DR287218FBW PC2-5300 CL5 (5-5-5)	VR5DR287218FBY/Z PC2-6400 CL5 (5-5-5) / PC2-6400 CL6 (6-6-6)	Unit
IDD0	765	765	810	810	mA
IDD1	855	855	900	900	mA
IDD2P	135	135	135	135	mA
IDD2Q	360	405	405	360	mA
IDD2N	360	405	405	450	mA
IDD3P-F	315	315	360	360	mA
IDD3P-S	162	162	162	162	mA
IDD3N	495	540	540	585	mA
IDD4R	1035	1170	1395	1395	mA
IDD4W	1035	1170	1395	1305	mA
IDD5	1890	1935	1980	1395	mA
IDD6	135	135	135	135	mA
IDD7	2340	2520	2700	2385	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 1Gbit

Symbol	VR5DR567218FBP PC2-3200 CL3 (3-3-3)	VR5DR567218FBS PC2-4200 CL4 (4-4-4)	VR5DR567218FBW PC2-5300 CL5 (5-5-5)	VR5DR567218FBY/Z PC2-6400 CL5 (5-5-5) / PC2-6400 CL6 (6-6-6)	Unit
IDD0	900	900	945	945	mA
IDD1	990	990	1035	1035	mA
IDD2P	270	270	270	270	mA
IDD2Q	720	810	810	720	mA
IDD2N	720	810	810	900	mA
IDD3P-F	360	360	720	720	mA
IDD3P-S	324	324	324	324	mA
IDD3N	990	1080	1080	1170	mA
IDD4R	1170	1305	1530	1530	mA
IDD4W	1170	1305	1530	1440	mA
IDD5	3780	3870	3960	2790	mA
IDD6	270	270	270	270	mA
IDD7	2475	2655	2835	2520	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 2Gb

Symbol	VR5DR127218GBP PC2-3200 CL3 (3-3-3)	VR5DR127218GBS PC2-4200 CL4 (4-4-4)	VR5DR127218GBW PC2-5300 CL5 (5-5-5)	VR5DR127218GBY/Z PC2-6400 CL5 (5-5-5) / PC2-6400 CL6 (6-6-6)	Unit
IDD0	882	882	918	963	mA
IDD1	1017	1017	1008	1053	mA
IDD2P	144	144	216	216	mA
IDD2Q	720	810	810	900	mA
IDD2N	810	900	900	990	mA
IDD3P-F	540	630	630	630	mA
IDD3P-S	180	180	324	324	mA
IDD3N	720	810	1260	1440	mA
IDD4R	1332	1422	3600	4320	mA
IDD4W	1197	1242	1773	2088	mA
IDD5	4500	4680	2088	2178	mA
IDD6	144	144	270	270	mA
IDD7	2727	2727	2628	2853	mA

AC INPUT TEST CONDITIONS

Parameter	Symbol	Value	Unit	Notes
Input reference voltage	VREF	0.50 * VDDQ	V	
Input signal maximum peak to peak swing	$V_{SWING\ (MAX)}$	1.0	V	
Input signal maximum slew rate	SLEW	1.0	V/ns	1, 2

Notes:

1. The Input signal minimum slew rate is to be maintain over the range from VIL(DC) max to VIL(AC) min for raising edges and the range from VIH(DC) min to VIL(AC) max for falling edges.
2. AC timings are reference with input waveforms switching from VIL(AC) to VIH(AC) on the positive transition and VIH(AC) to VIL(AC) on the negative transitions.

AC OPERATING CONDITIONS (VDD = 1.8V ± 0.1V, TOPR = 0 to 85 °C)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Input Differential Voltage	VID(ac)	0.5	VDDQ +0.6	V	1
Input Crossing Point Voltage	VIX(ac)	0.5*VDDQ -0.175	0.5*VDDQ +0.175	V	2

Notes:

1. VID (AC) specifies the input differential voltage I Vtr – Vcp I required for switching, where Vtr is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and Vcp is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to VIH (AC) – VIL (AC).
2. The typical value of Vix (AC) is expected to be about 0.5 x VDDQ of the transmitting devices and Vix (AC) is expected to track variations in VDDQ.

OCD Default Characteristics

Description	Min	Nom	Max	Unit	Notes
Output Impedance	12.6	18	23.4	Ohms	1, 2
Pull-Up and Pull-Down mismatch	0	-	4	Ohms	1, 2, 3
Output slew rate	1.5	-	4.5	V/ns	1, 4, 5

Notes:

1. Absolute specifications: 0°C ≤ Tcase ≤ 85°C; VDD = 1.8V +/- 0.1V, VDDQ = 1.8V +/- 0.1V.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Symbol	Parameter	PC2-3200		PC2-4200		PC2-5300		PC2-6400		Units
		min	max	min	max	min	max	min	max	
tAC	DQ output access time from CK/CK	-600	+600	-500	+500	-450	+450	- 400	400	ps
tDQSCK	DQS output access time from CK/CK	-500	+500	-450	+450	-400	+400	- 350	350	ps
tCH	CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tHP	CK half period	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ps
tCK	Clock cycle time, CL=x	5000	8000	3750	8000	3000	8000	2500	8000	ps
tDH(base)	DQ and DM input hold time	275	x	225	x	175	x	125	x	ps
tDS(base)	DQ and DM input setup time	150	x	100	x	100	x	50	x	ps
tIPW	Control & Address input pulse width for each input	0.6	x	0.6	x	0.6	x	0.6	x	tCK
tDIPW	DQ and DM input pulse width for each input	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tHZ	Data-out high-impedance time from CK/CK	x	tAC max	x	tAC max	x	tAC max	x	tAC max	ps
tLZ(DQS)	DQS low-impedance time from CK/CK	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
tLZ(DQ)	DQ low-impedance time from CK/CK	2*tACmin	tAC max	2*tACmin	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	ps
tDQSQ	DQS-DQ skew for DQS and associated DQ signals	x	350	x	300	x	240	x	200	ps
tQHS	DQ hold skew factor	x	450	x	400	x	340	x	300	ps
tQH	DQ/DQS output hold time from DQS	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps
tDQSS	First DQS latching transition to associated clock edge	-0.25	0.25	-0.25	0.25	-0.25	0.25	- 0.25	0.25	tCK
tDQSH	DQS input high pulse width	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tDQSL	DQS input low pulse width	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tDSS	DQS falling edge to CK setup time	0.2	x	0.2	x	0.2	x	0.2	x	tCK
tDSH	DQS falling edge hold time from CK	0.2	x	0.2	x	0.2	x	0.2	x	tCK
tMRD	Mode register set command cycle time	2	x	2	x	2	x	2	x	tCK
tWPST	Write postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tWPRE	Write preamble	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tIH(base)	Address and control input hold time	475	x	375	x	275	x	250	x	ps
tIS(base)	Address and control input setup time	350	x	250	x	200	x	175	x	ps
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tRRD	Active to active command period for 1kb page size products	7.5	x	7.5	x	7.5	x	7.5	x	ns
tRRD	Active to active command period for 2kb page size products	10	x	10	x	10	x	10	x	ns
tFAW	Four Bank Activate period for 1kb page size products	37.5		37.5		37.5		35		ns
tFAW	Four Bank Activate period for 2kb page size products	50		50		50		45		ns
tCCD	CAS to CAS command delay	2		2		2		2	x	tCK
tWR	Write recovery time	15	x	15	x	15	x	15	x	ns

AC CHARACTERISTICS

Symbol	Parameter		PC2-3200		PC2-4200		PC2-5300		PC2-6400		Units
			min	max	min	max	min	max	min	max	
tRC	Active to Active/Auto-Refresh command period	CL = 3	55	-	-	-	-	-	-	-	ns
		CL = 4	-		60		-		-		
		CL = 5	-		-		60		57.5		
		CL = 6	-		-		-		60		
tRFC	Auto-Refresh to Active/Auto-Refresh command period	256Mb, 512Mb	105	70000	105	70000	105	70000	105	70000	ns
		1Gb	127.5		127.5		127.5		127.5		
		2Gb	195		195		195		195		
tRCD	Active to Read or Write (with and without Auto-Precharge) delay	CL = 3	15	-	-	-	-	-	-	-	ns
		CL = 4	-		15		-		-		
		CL = 5	-		-		15		12.5		
		CL = 6	-		-		-		15		
tRP	Precharge command period	CL = 3	15	-	-	-	-	-	-	-	ns
		CL = 4	-		15		-		-		
		CL = 5	-		-		15		12.5		
		CL = 6	-		-		-		15		
tRAS	Active to Precharge command	CL = 3	40	70000	-	70000	-	70000	-	70000	ns
		CL = 4	-		45		-		-		
		CL = 5	-		-		45		45		
		CL = 6	-		-		-		45		
tDAL	Auto precharge write recovery + precharge time		WR+tRP	x	WR+tRP	x	WR+tRP	x	WR+tRP	x	tCK
tWTR	Internal write to read command delay		10	x	7.5	x	7.5	x	7.5		ns
tRTP	Internal read to precharge command delay		7.5		7.5		7.5		7.5		ns
tXSNR	Exit self refresh to a non-read command		tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns
tXSRD	Exit self refresh to a read command		200		200		200		200	x	tCK
tXP	Exit precharge power down to any non-read command		2	x	2	x	2	x	2	x	tCK
tXARD	Exit active power down to read command		2	x	2	x	2	x	2	x	tCK
tXARDS	Exit active power down to read command (slow exit, lower power)		6 - AL		6 - AL		7 - AL		8 - AL		tCK
^{t}CKE	CKE minimum pulse width (high and low pulse width)		3		3		3		3		tCK
^{t}AOND	ODT turn-on delay		2	2	2	2	2	2	2	2	tCK
^{t}AON	ODT turn-on		tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +0.7	tAC(min)	tAC(max) + 0.7	ns
^{t}AONPD	ODT turn-on(Power-Down mode)		tAC(min)+ 2	2tCK+tAC (max)+1	tAC(min)+ 2	2tCK+tAC (max)+1	tAC(min)+ 2	2tCK+tAC (max)+1	tAC(min)+ 2	2tCK+tAC (max)+1	ns
^{t}AOFD	ODT turn-off delay		2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK
^{t}AOF	ODT turn-off		tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns
^{t}AOFPD	ODT turn-off (Power-Down mode)		tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK + tAC(max) +1	ns
tANPD	ODT to power down entry latency		3		3		3		3		tCK
tAXPD	ODT power down exit latency		8		8		8		8		tCK
tOIT	OCD drive mode output delay		0	12	0	12	0	12	0	12	ns
tDelay	Minimum time clocks remain ON after CKE asynchronously drops LOW		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns

REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	August 15, 2007	Initial Release, conversion of PS5DRXX7218EBX to include 1Gb device configurations	Brian Ouellette
B	November 28, 2007	Correct Pins 198 and 200. Update dual rank mechanical outline.	Brian Ouellette
C	May 30, 2008	Add DDR2-800 configurations	Brian Ouellette
D	June 2, 2008	Remove SA2 from Pin Function table, correct SA2 on block diagrams.	Brian Ouellette
E	April 28, 2009	Add 2Gb configurations	Brian Ouellette
E1	November 23, 2011	Add new logo and company name	
F	February 2, 2018	Add new logo and company name	

STATEMENT OF COMPLIANCE

Viking Technology (tm), Sanmina-SCI Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.