MODULE CONFIGURATIONS – NON-ECC

Viking Part Number	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR5EU646418EBP	512MB	64MX64	64M x 8 (8)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5EU646418EBS	512MB	64MX64	64M x 8 (8)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5EU646418EBW	512MB	64MX64	64M x 8 (8)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5EU646418EBY	512MB	64MX64	64M x 8 (8)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5EU286418EBP	1GB	128MX64	64M x 8 (16)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU286418EBS	1GB	128MX64	64M x 8 (16)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU286418EBW	1GB	128MX64	64M x 8 (16)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5EU286418EBY	1GB	128MX64	64M x 8 (16)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5EU286418FBP	1GB	128MX64	128M x 8 (8)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5EU286418FBS	1GB	128MX64	128M x 8 (8)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5EU286418FBW	1GB	128MX64	128M x 8 (8)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5EU286418FBY	1GB	128MX64	128M x 8 (8)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5EU286418FBZ	1GB	128MX64	128M x 8 (8)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5EU286418FBA	1GB	128MX64	128M x 8 (8)	FBGA	1	PC2-8500	CL7 (7-7-7)
VR5EU566418FBP	2GB	256MX64	128M x 8 (16)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU566418FBS	2GB	256MX64	128M x 8 (16)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU566418FBW	2GB	256MX64	128M x 8 (16)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5EU566418FBY	2GB	256MX64	128M x 8 (16)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5EU566418FBZ	2GB	256MX64	128M x 8 (16)	FBGA	2	PC2-6400	CL6 (6-6-6)
VR5EU566418FBA	2GB	256MX64	128M x 8 (16)	FBGA	2	PC2-8500	CL7 (7-7-7)
VR5EU566418GBP	2GB	256MX64	256M x 8 (8)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5EU566418GBS	2GB	256MX64	256M x 8 (8)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5EU566418GBW	2GB	256MX64	256M x 8 (8)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5EU566418GBY	2GB	256MX64	256M x 8 (8)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5EU566418GBZ	2GB	256MX64	256M x 8 (8)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5EU126418GBP	4GB	512MX64	256M x 8 (16)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU126418GBS	4GB	512MX64	256M x 8 (16)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU126418GBW	4GB	512MX64	256M x 8 (16)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5EU126418GBY	4GB	512MX64	256M x 8 (16)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5EU126418GBZ	4GB	512MX64	256M x 8 (16)	FBGA	2	PC2-6400	CL6 (6-6-6)

Pb-FREE

MODULE CONFIGURATIONS - ECC

Viking Part Number	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR5EU647218EBP	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5EU647218EBS	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5EU647218EBW	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5EU647218EBY	512MB	64Mx72	64M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5EU287218EBP	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU287218EBS	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU287218EBW	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5EU287218EBY	1GB	128Mx72	64M x 8 (18)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5EU287218FBP	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5EU287218FBS	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5EU287218FBW	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5EU287218FBY	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5EU287218FBZ	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5EU287218FBA	1GB	128Mx72	128M x 8 (9)	FBGA	1	PC2-8500	CL7 (7-7-7)
VR5EU567218FBP	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU567218FBS	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU567218FBW	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5EU567218FBY	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5EU567218FBZ	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-6400	CL6 (6-6-6)
VR5EU567218FBA	2GB	256Mx72	128M x 8 (18)	FBGA	2	PC2-8500	CL7 (7-7-7)
VR5EU567218GBP	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5EU567218GBS	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5EU567218GBW	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5EU567218GBY	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-6400	CL5 (5-5-5)
VR5EU567218GBZ	2GB	256Mx72	256M x 8 (9)	FBGA	1	PC2-6400	CL6 (6-6-6)
VR5EU127218GBP	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU127218GBS	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU127218GBW	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5EU127218GBY	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-6400	CL5 (5-5-5)
VR5EU127218GBZ	4GB	512Mx72	256M x 8 (18)	FBGA	2	PC2-6400	CL6 (6-6-6)

Features

- 240 pin Unbuffered DIMM
- Single 1.8V ± 0.1V Power Supply
- Burst Length (4, 8)
- Burst type (Sequential & Interleave)
- Auto & Self-Refresh.
- 8k/64ms Refresh Period.
- Differential CLK (#CLK) input.
- On-die termination (ODT)
- Off-chip driver (OCD) impedance calibration
- Serial Presence Detect with EEPROM.
- RoHS Compliant* (see last page)

PIN CONFIGURATIONS

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VREF	121	VSS	31	DQ19	151	VSS	61	A4	181	VDDQ	91	VSS	211	DM5
2	VSS	122	DQ4	32	VSS	152	DQ28	62	VDDQ	182	A3	92	/DQS5	212	*/DQS14
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	VSS
4	DQ1	124	VSS	34	DQ25	154	VSS	64	VDD	184	VDD	94	VSS	214	DQ46
5	VSS	125	DM0	35	VSS	155	DM3	65	VSS	185	CK0	95	DQ42	215	DQ47
6	/DQS0	126	*/DQS9	36	/DQS3	156	*/DQS12	66	VSS	186	/CK0	96	DQ43	216	VSS
7	DQS0	127	VSS	37	DQS3	157	VSS	67	VDD	187	VDD	97	VSS	217	DQ52
8	VSS	128	DQ6	38	VSS	158	DQ30	68	*PAR_IN	188	A0	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	69	VDD	189	VDD	99	DQ49	219	VSS
10	DQ3	130	VSS	40	DQ27	160	VSS	70	A10/AP	190	BA1	100	VSS	220	CK2
11	VSS	131	DQ12	41	VSS	161	§CB4	71	BA0	191	VDDQ	101	SA2	221	/CK2
12	DQ8	132	DQ13	42	§CB0	162	§CB5	72	VDDQ	192	/RAS	102	NC	222	VSS
13	DQ9	133	VSS	43	§CB1	163	VSS	73	/WE	193	/S0	103	VSS	223	DM6
14	VSS	134	DM1	44	VSS	164	§DM8	74	/CAS	194	VDDQ	104	/DQS6	224	*/DQS15
15	/DQS1	135	*/DQS10	45	§/DQS8	165	*/DQS17	75	VDDQ	195	ODT0	105	DQS6	225	VSS
16	DQS1	136	VSS	46	§DQS8	166	VSS	76	**/S1	196	†A13	106	VSS	226	DQ54
17	VSS	137	CK1	47	VSS	167	§CB6	77	**ODT1	197	VDD	107	DQ50	227	DQ55
18	*/RESET	138	/CK1	48	§CB2	168	§CB7	78	VDDQ	198	VSS	108	DQ51	228	VSS
19	NC	139	VSS	49	§CB3	169	VSS	79	VSS	199	DQ36	109	VSS	229	DQ60
20	VSS	140	DQ14	50	VSS	170	VDDQ	80	DQ32	200	DQ37	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	VDDQ	171	**CKE1	81	DQ33	201	VSS	111	DQ57	231	VSS
22	DQ11	142	VSS	52	CKE0	172	VDD	82	VSS	202	DM4	112	VSS	232	DM7
23	VSS	143	DQ20	53	VDD	173	*A15	83	/DQS4	203	*/DQS13	113	/DQS7	233	*/DQS16
24	DQ16	144	DQ21	54	†BA2	174	†A14	84	DQS4	204	VSS	114	DQS7	234	VSS
25	DQ17	145	VSS	55	*ERR_OUT	175	VDDQ	85	VSS	205	DQ38	115	VSS	235	DQ62
26	VSS	146	DM2	56	VDDQ	176	A12	86	DQ34	206	DQ39	116	DQ58	236	DQ63
27	/DQS2	147	*/DQS11	57	A11	177	A9	87	DQ35	207	VSS	117	DQ59	237	VSS
28	DQS2	148	VSS	58	A7	178	VDD	88	VSS	208	DQ44	118	VSS	238	VDDSPD
29	VSS	149	DQ22	59	VDD	179	A8	89	DQ40	209	DQ45	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	90	DQ41	210	VSS	120	SCL	240	SA1

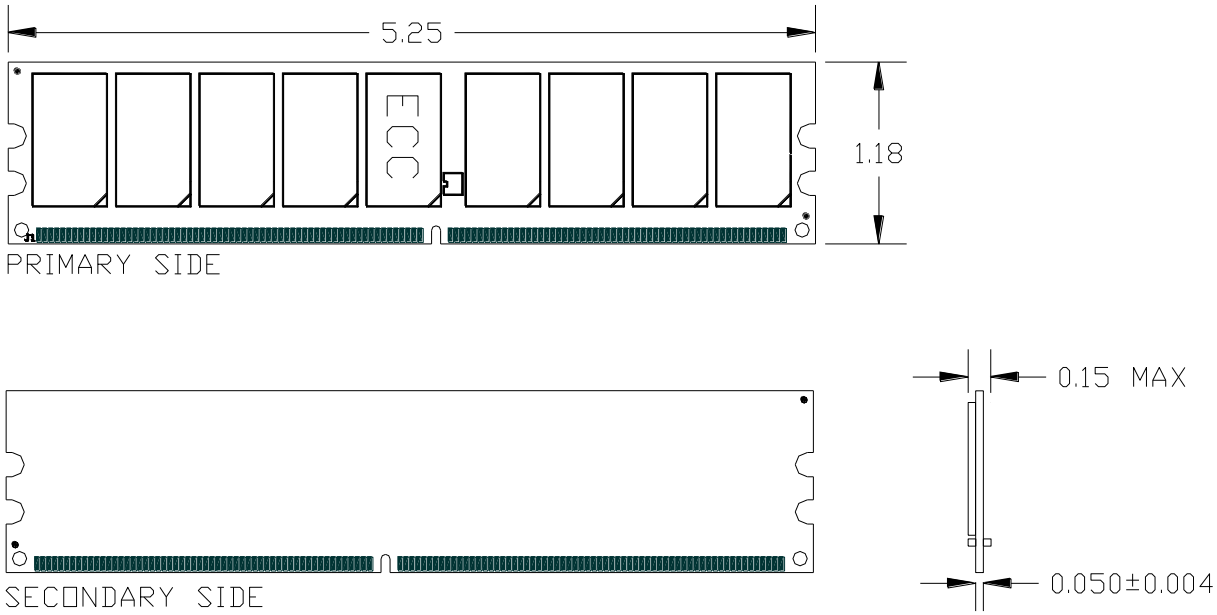
* Pins are not used in this module
§ Pins are used for ECC modules
** Pins are used for 2 rank modules
† BA2 & A13 used for 1Gb based module. BA2, A13 & A14 used for 2Gb based module.

PIN FUNCTION DESCRIPTION

SYMBOL	TYPE	POLARITY	DESCRIPTION
CK0, CK1 /CK0, /CK1	IN	Positive Edge Negative Edge	Clock: CK and /CK are differential clock inputs. All addresses and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output data (DQs, DQS and /DQS) is referenced to the crossings of CK and /CK.
CKE0 ~ CKE1	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
/S0 ~ /S1	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both S[0:1] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state.
ODT0 ~ ODT1	IN	Active High	On-Die Termination control signals
/RAS, /CAS, /WE	IN	Active Low	CAS, WE When sampled at the positive rising edge of the clock, /CAS, /RAS, and /WE define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL18 inputs
VDD	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA [2:0]	IN	-	Selects which SDRAM bank of four or eight is activated.
A [14:0]	IN	-	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, and BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ [63:0]	I/O	-	Data Input/Output pins
DM [8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
VDD, GND	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
DQS [7:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
/DQS [7:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
/EVENT	Out	-	The optional EVENT pin is reserved for use to flag critical module temperatures and is used in conjunction with a SPD temperature sensing option.
SA [1:0]	IN	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDDSPD on the system planar to act as a pull-up.
VDDSPD	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector, which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operations.

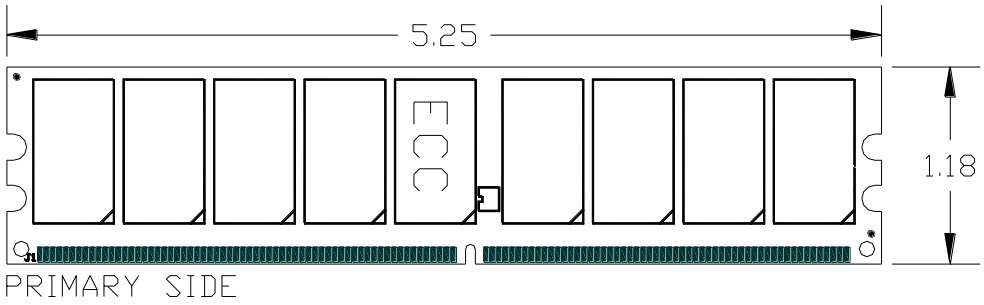
MECHANICAL OUTLINE SINGLE RANK

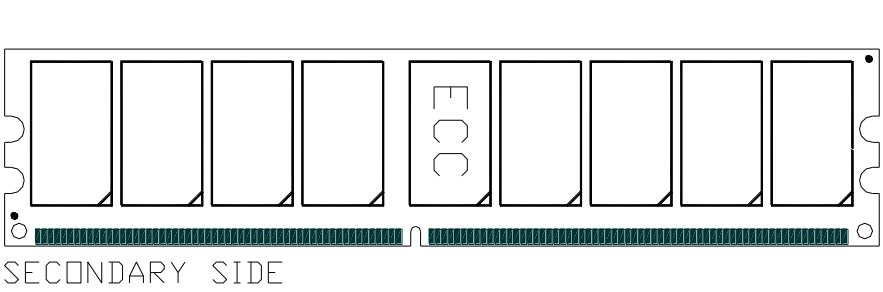
All dimensions are in inches with a tolerance of +/- 0.005 unless otherwise specified.

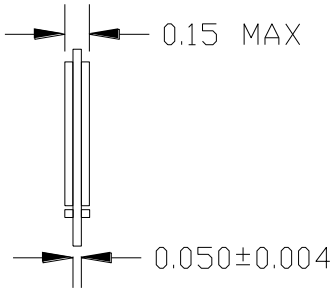


MECHANICAL OUTLINE DUAL RANK

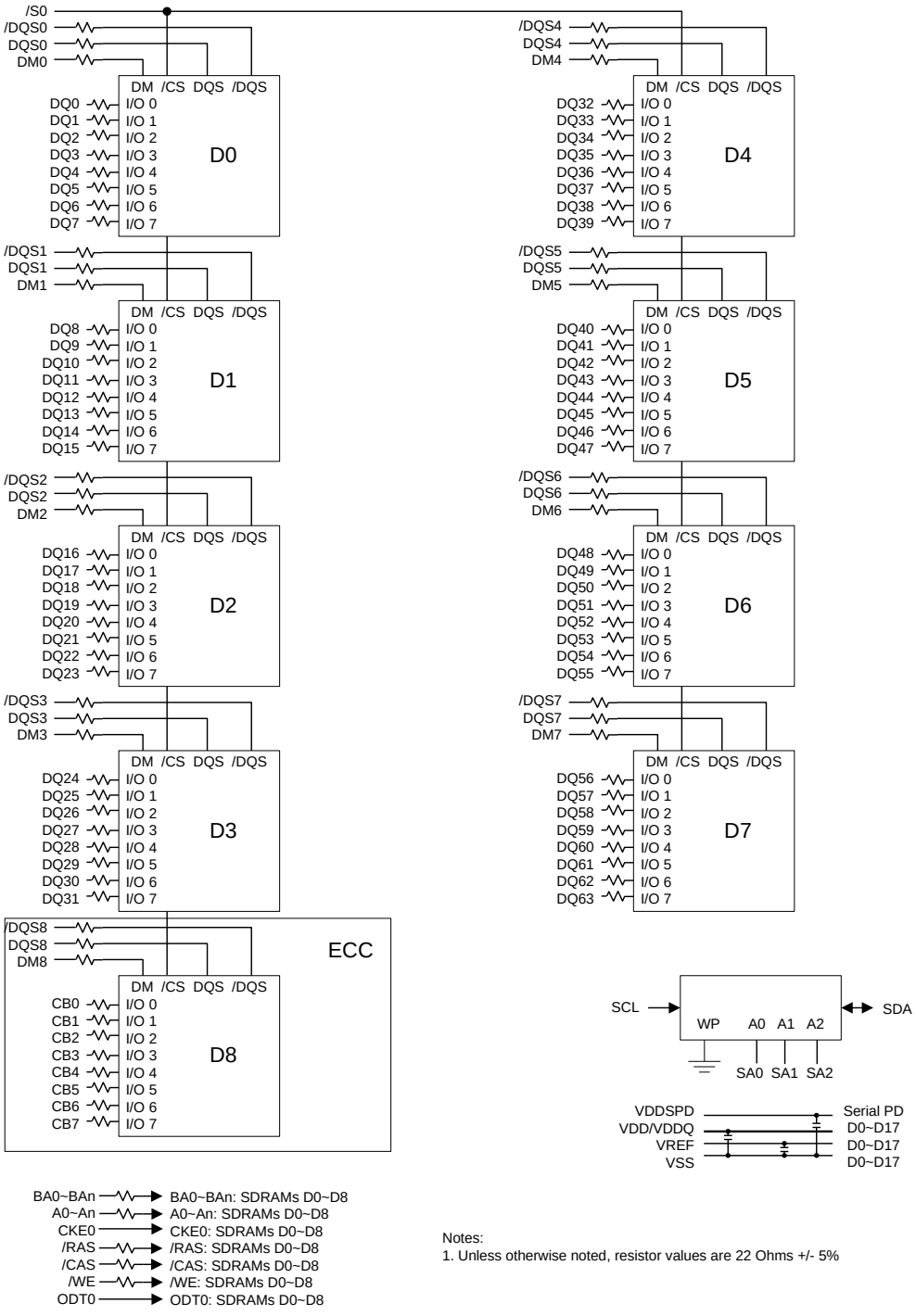
All dimensions are in inches with a tolerance of +/- 0.005 unless otherwise specified.





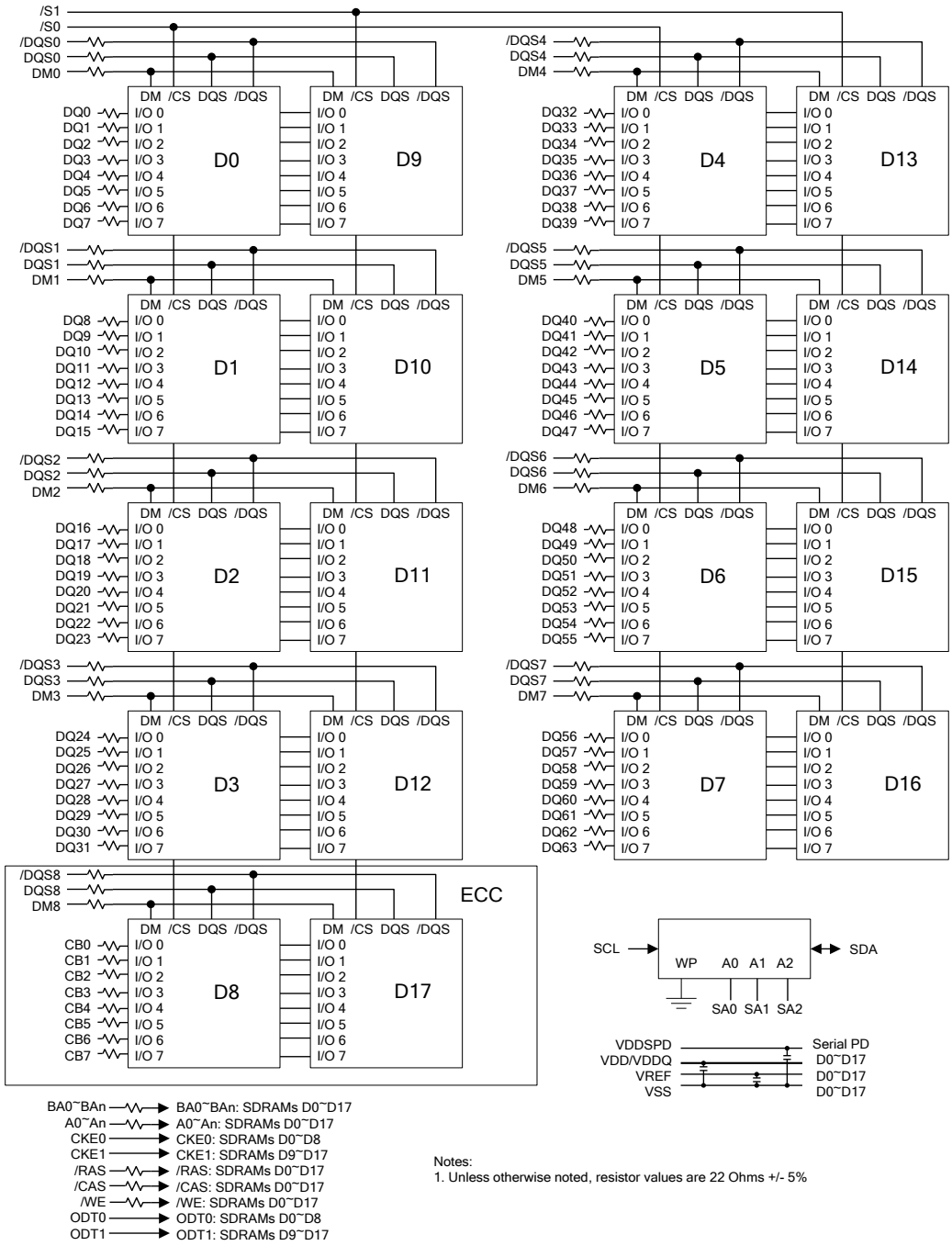


FUNCTIONAL BLOCK DIAGRAM SINGLE RANK



Notes:
1. Unless otherwise noted, resistor values are 22 Ohms +/- 5%

FUNCTIONAL BLOCK DIAGRAM DUAL RANK



Notes:
1. Unless otherwise noted, resistor values are 22 Ohms +/- 5%

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND	Vin, Vout	-0.5 ~ 2.3	V
Voltage on VDD supply relative to GND	VDD	-1.0 ~ 2.3	V
Voltage on VDDQ supply relative to GND	VDDQ	-0.5 ~ 2.3	V
Storage temperature	TSTG	-55 ~ +100	°C

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_1.8)

Recommended operating conditions (Voltages referenced to GND, Tcase = 0 to 85°C)

Parameter		Symbol	Min.	Max.	Unit	Notes
Case Temperature		Tcase	0	85	ºC	
Supply voltage		VDD	1.7	1.9	V	
Supply voltage for DQ, DQS		VDDQ	1.7	1.9	V	
Input reference voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	1, 2
EEPROM Supply Voltage		VDDSPD	1.7	3.6	V	
Input high voltage		VIH	VREF + 0.125	VDDQ + 0.3	V	
Input low voltage		VIL	-0.3	VREF - 0.125	V	
Input leakage current Non-ECC	Single Rank	IIL	-40	40	µA	3
	Dual Rank	IIL	-80	80	µA	3
Input leakage current ECC	Single Rank	IIL	-45	45	µA	3
	Dual Rank	IIL	-90	90	µA	3
Output leakage current	Single Rank	IOL	-5	5	µA	4
	Dual Rank	IOL	-10	10	µA	4

Note: 1. Peak to peak AC noise on VREF may not exceed +/- 2% VREF (DC). VREF is also expected to track noise variation in VDD.
2. For any pin under test input of 0 V ≤ VIN ≤ VDDQ +0.3 V.
3. Any input 0V≤Vin≤VDD; all other pins not under test = 0V.
4. 0V≤VOUT≤VDDQ; DQ and ODT disabled

CAPACITANCE (VDD = 1.8V, TA = 25ºC)

Parameter		Symbol	Min		Max		Unit
			Single Rank	Dual Ranks	Single Rank	Dual Ranks	
Input capacitance, Non-ECC (A0 ~ An, BA0 ~ BA1)		CIN1	13	21	21	37	pF
Input capacitance, Non-ECC (/RAS, /CAS, /WE)		CIN2	13	21	21	37	pF
Input capacitance, Non-ECC (CKE0 ~ *CKE1)		CIN3	13		21		pF
Input capacitance, Non-ECC (/S0 ~*/S1)		CIN4	13		21		pF
Input capacitance, ECC (A0 ~ An, BA0 ~ BA1)		CIN1	14	23	23	41	pF
Input capacitance, ECC (/RAS, /CAS, /WE)		CIN2	14	23	23	41	pF
Input capacitance, ECC (CKE0 ~ *CKE1)		CIN3	14		23		pF
Input capacitance, ECC (/S0 ~*/S1)		CIN4	14		23		pF
Input capacitance (CK0, /CK0 ~ CK1, /CK1)		CIN5a	8	11	11	17	pF
Input capacitance (DQS0 ~ DQS7, /DQS0 ~ /DQS7), (DM0 ~ DM7)	400MHz, 533MHz	CIN6a	7.5	10	9	13	pF
	667MHz, 800MHz	CIN6c	7.5	10	8.5	12.5	pF
Data input/output capacitance (DQ0 ~ DQ63, CB0 ~ CB7)	400MHz, 533MHz	COUTa	7.5	10	9	13	pF
	667MHz, 800MHz	COUTc	7.5	10	8.5	12.5	pF

*Used in dual ranked module only

Parameter	Symbol	Test Condition		Unit	Note
Operating one bank active-precharge current	IDD0	tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 2
Operating one bank active-read-precharge current	IDD1	IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	1, 2
Precharge power-down current	IDD2P	All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	1, 3
Precharge quiet standby current	IDD2Q	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	1, 3
Precharge standby current	IDD2N	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 3
Active power-down current	IDD3P-F	All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MR(12) = 0	mA	1, 3
	IDD3P-S		Slow PDN Exit MR(12) = 1		
Active standby current	IDD3N	All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 3
Operating burst read current	IDD4R	All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	1, 2
Operating burst write current	IDD4W	All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 2
Auto refresh current	IDD5	tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	1, 3
Self refresh current	IDD6	CK and /CK at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		mA	1, 3
Operating bank interleave read current	IDD7	All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R		mA	1, 2

DC CHARACTERISTICS DEFINITIONS (Recommended operating conditions unless otherwise noted, Tcase = 0 to 85 °C)

Note:

1. Calculated values are from component data. ODT disabled. IDD1 and IDD4R are defined with the outputs disabled. Currents are for DDR2 SDRAM components only.
2. Inactive ranks are in IDD2P Precharge Power-Down Standby Current mode.
3. All ranks are in the same IDD current mode.

DC CHARACTERISTICS CURRENTS SINGLE RANK 512Mbit – Non-ECC

Symbol	VR5EU646418EBP PC2-3200 CL3 (3-3-3)	VR5EU646418EBS PC2-4200 CL4 (4-4-4)	VR5EU646418EBW PC2-5300 CL5 (5-5-5)	VR5EU646418EBY PC2-6400 CL5 (5-5-5)	Unit
IDD0	640	640	680	800	mA
IDD1	760	760	800	920	mA
IDD2P	64	64	64	56	mA
IDD2Q	240	240	280	400	mA
IDD2N	280	280	320	440	mA
IDD3P-F	240	240	240	320	mA
IDD3P-S	96	96	96	96	mA
IDD3N	400	400	440	560	mA
IDD4R	880	1000	1160	1640	mA
IDD4W	880	960	1120	1560	mA
IDD5	1120	1120	1200	1840	mA
IDD6	64	64	64	56	mA
IDD7	1760	1760	1760	2400	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 512Mbit - ECC

Symbol	VR5EU647218EBP PC2-3200 CL3 (3-3-3)	VR5EU647218EBS PC2-4200 CL4 (4-4-4)	VR5EU647218EBW PC2-5300 CL5 (5-5-5)	VR5EU647218EBY PC2-6400 CL5 (5-5-5)	Unit
IDD0	720	720	765	900	mA
IDD1	855	855	900	1035	mA
IDD2P	72	72	72	63	mA
IDD2Q	270	270	315	450	mA
IDD2N	315	315	360	495	mA
IDD3P-F	270	270	270	360	mA
IDD3P-S	108	108	108	108	mA
IDD3N	450	450	495	630	mA
IDD4R	990	1125	1305	1845	mA
IDD4W	990	1080	1260	1755	mA
IDD5	1260	1260	1350	2070	mA
IDD6	72	72	72	63	mA
IDD7	1980	1980	1980	2700	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 1Gbit – Non-ECC

Symbol	VR5EU286418FBP PC2-3200 CL3	VR5EU286418FBS PC2-4200 CL4	VR5EU286418FBW PC2-5300 CL5	VR5EU286418FBY/Z PC2-6400 CL5/6	VR5EU286418FBA PC2-8500 CL7	Unit
IDD0	680	680	720	720	920	mA
IDD1	760	760	800	880	1040	mA
IDD2P	120	120	120	56	56	mA
IDD2Q	320	360	360	400	480	mA
IDD2N	320	360	360	400	480	mA
IDD3P-F	280	280	320	320	400	mA
IDD3P-S	144	144	144	80	80	mA
IDD3N	440	480	480	480	560	mA
IDD4R	920	1040	1240	1280	1680	mA
IDD4W	920	1040	1240	1280	1680	mA
IDD5	1680	1720	1760	1880	2120	mA
IDD6	120	120	120	56	56	mA
IDD7	2080	2240	2400	2680	3400	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 1Gbit - ECC

Symbol	VR5EU287218FBP PC2-3200 CL3	VR5EU287218FBS PC2-4200 CL4	VR5EU287218FBW PC2-5300 CL5	VR5EU287218FBY/Z PC2-6400 CL5/6	VR5EU287218FBA PC2-8500 CL7	Unit
IDD0	765	765	810	810	1035	mA
IDD1	855	855	900	990	1170	mA
IDD2P	135	135	135	53	63	mA
IDD2Q	360	405	405	450	540	mA
IDD2N	360	405	405	450	540	mA
IDD3P-F	315	315	360	360	450	mA
IDD3P-S	162	162	162	90	90	mA
IDD3N	495	540	540	540	630	mA
IDD4R	1035	1170	1395	1440	1890	mA
IDD4W	1035	1170	1395	1440	1890	mA
IDD5	1890	1935	1980	2115	2385	mA
IDD6	135	135	135	53	63	mA
IDD7	2340	2520	2700	3015	3825	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 2Gb – Non-ECC

Symbol	VR5EU566418GBP PC2-3200 CL3 (3-3-3)	VR5EU566418GBS PC2-4200 CL4 (4-4-4)	VR5EU566418GBW PC2-5300 CL5 (5-5-5)	VR5EU566418GBY/Z PC2-6400 CL5/6	Unit
IDD0	568	600	648	696	mA
IDD1	600	640	688	728	mA
IDD2P	128	128	128	128	mA
IDD2Q	352	392	440	488	mA
IDD2N	360	400	464	504	mA
IDD3P-F	240	256	264	280	mA
IDD3P-S	136	136	136	136	mA
IDD3N	416	456	504	552	mA
IDD4R	928	976	1040	1144	mA
IDD4W	880	992	1112	1232	mA
IDD5	1616	1680	1720	1776	mA
IDD6	128	128	128	128	mA
IDD7	1456	1472	1512	1648	mA

DC CHARACTERISTICS CURRENTS SINGLE RANK 2Gb - ECC

Symbol	VR5EU567218GBP PC2-3200 CL3 (3-3-3)	VR5EU567218GBS PC2-4200 CL4 (4-4-4)	VR5EU567218GBW PC2-5300 CL5 (5-5-5)	VR5EU567218GBY/Z PC2-6400 CL5/6	Unit
IDD0	639	675	729	783	mA
IDD1	675	720	774	819	mA
IDD2P	144	144	144	144	mA
IDD2Q	396	441	495	549	mA
IDD2N	405	450	522	567	mA
IDD3P-F	270	288	297	315	mA
IDD3P-S	153	153	153	153	mA
IDD3N	468	513	567	621	mA
IDD4R	1044	1098	1170	1287	mA
IDD4W	990	1116	1251	1386	mA
IDD5	1818	1890	1935	1990	mA
IDD6	144	144	144	144	mA
IDD7	1638	1656	1701	1854	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 512Mbit – Non-ECC

Symbol	VR5EU286418EBP PC2-3200 CL3 (3-3-3)	VR5EU286418EBS PC2-4200 CL4 (4-4-4)	VR5EU286418EBW PC2-5300 CL5 (5-5-5)	VR5EU286418EBY PC2-6400 CL5 (5-5-5)	Unit
IDD0	824	960	1000	856	mA
IDD1	944	1080	1120	976	mA
IDD2P	128	160	160	112	mA
IDD2Q	320	400	400	800	mA
IDD2N	400	480	560	880	mA
IDD3P-F	560	640	640	640	mA
IDD3P-S	320	400	400	192	mA
IDD3N	960	1040	1120	1120	mA
IDD4R	1264	1600	1920	1696	mA
IDD4W	1264	1600	1840	1616	mA
IDD5	3680	4000	4320	3680	mA
IDD6	96	96	96	112	mA
IDD7	2464	2640	2640	2456	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 512Mbit - ECC

Symbol	VR5EU287218EBP PC2-3200 CL3 (3-3-3)	VR5EU287218EBS PC2-4200 CL4 (4-4-4)	VR5EU287218EBW PC2-5300 CL5 (5-5-5)	VR5EU287218EBY PC2-6400 CL5 (5-5-5)	Unit
IDD0	927	1080	1125	963	mA
IDD1	1062	1215	1260	1098	mA
IDD2P	144	180	180	126	mA
IDD2Q	360	450	450	900	mA
IDD2N	450	540	630	990	mA
IDD3P-F	630	720	720	720	mA
IDD3P-S	360	450	450	216	mA
IDD3N	1080	1170	1260	1260	mA
IDD4R	1422	1800	2160	1908	mA
IDD4W	1422	1800	2070	1818	mA
IDD5	4140	4500	4860	4140	mA
IDD6	108	108	108	126	mA
IDD7	2772	2970	2970	2763	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 1Gbit – Non-ECC

Symbol	VR5EU566418FBP PC2-3200 CL3	VR5EU566418FBS PC2-4200 CL4	VR5EU566418FBW PC2-5300 CL5	VR5EU566418FBY/Z PC2-6400 CL5/6	VR5EU566418FBA PC2-6400 CL7	Unit
IDD0	800	800	840	776	976	mA
IDD1	800	880	920	936	1096	mA
IDD2P	240	240	240	112	112	mA
IDD2Q	640	720	720	800	960	mA
IDD2N	640	720	720	800	960	mA
IDD3P-F	320	320	640	640	800	mA
IDD3P-S	288	288	288	160	160	mA
IDD3N	880	960	960	960	1120	mA
IDD4R	1040	1160	1360	1336	1736	mA
IDD4W	1040	1160	1360	1336	1736	mA
IDD5	3360	3440	3520	3760	4240	mA
IDD6	240	240	240	112	112	mA
IDD7	2200	2360	2520	2736	3456	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 1Gb - ECC

Symbol	DDR2-800	DDR2-677				Unit
IDD0	882	810				mA
IDD1	972	900				mA
IDD2P	180	180				mA
IDD2Q	432	432				mA
IDD2N	504	486				mA
IDD3P-F	360	270				mA
IDD3P-S	180	180				mA
IDD3N	594	540				mA
IDD4R	1377	1260				mA
IDD4W	1422	1305				mA
IDD5	1602	1530				mA
IDD6	180	180				mA
IDD7	2187	1935				mA

DC CHARACTERISTICS CURRENTS DUAL RANK 2Gb – Non-ECC

Symbol	VR5EU126418GBP PC2-3200 CL3 (3-3-3)	VR5EU126418GBS PC2-4200 CL4 (4-4-4)	VR5EU126418GBW PC2-5300 CL5 (5-5-5)	VR5EU126418GBY/Z PC2-6400 CL5/6	Unit
IDD0	568	728	776	824	mA
IDD1	728	768	816	856	mA
IDD2P	256	256	256	256	mA
IDD2Q	704	784	880	976	mA
IDD2N	720	800	928	1008	mA
IDD3P-F	480	512	528	560	mA
IDD3P-S	272	272	272	272	mA
IDD3N	832	912	1008	1104	mA
IDD4R	1056	1104	1168	1272	mA
IDD4W	1008	1120	1240	1360	mA
IDD5	3232	3360	3440	3552	mA
IDD6	256	256	256	256	mA
IDD7	1584	1600	1640	1776	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 2Gb - ECC

Symbol	VR5EU127218GBP PC2-3200 CL3 (3-3-3)	VR5EU127218GBS PC2-4200 CL4 (4-4-4)	VR5EU127218GBW PC2-5300 CL5 (5-5-5)	VR5EU127218GBY/Z PC2-6400 CL5/6	Unit
IDD0	783	819	873	927	mA
IDD1	819	864	918	963	mA
IDD2P	288	288	288	288	mA
IDD2Q	792	882	990	1098	mA
IDD2N	810	900	1044	1134	mA
IDD3P-F	540	576	594	630	mA
IDD3P-S	306	306	306	306	mA
IDD3N	936	1026	1134	1242	mA
IDD4R	1188	1242	1314	1431	mA
IDD4W	1134	1260	1395	1530	mA
IDD5	3636	3780	3870	3980	mA
IDD6	288	288	288	288	mA
IDD7	1782	1800	1845	1998	mA

AC INPUT TEST CONDITIONS

Parameter	Symbol	Value	Unit	Notes
Input reference voltage	VREF	0.50 * VDDQ	V	
Input signal maximum peak to peak swing	VSWING (MAX)	1.0	V	
Input signal maximum slew rate	SLEW	1.0	V/ns	1, 2

Notes:

1. The Input signal minimum slew rate is to be maintain over the range from VIL(DC) max to VIL(AC) min for raising edges and the range from VIH(DC) min to VIL(AC) max for falling edges.
2. AC timings are reference with input waveforms switching from VIL(AC) to VIH(AC) on the positive transition and VIH(AC) to VIL(AC) on the negative transitions.

AC OPERATING CONDITIONS (VDD = 1.8V ± 0.1V, TOPR = 0 to 85 °C)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Input Differential Voltage	VID(ac)	0.5	VDDQ +0.6	V	1
Input Crossing Point Voltage	VIX(ac)	0.5*VDDQ -0.175	0.5*VDDQ +0.175	V	2

Notes:

1. VID (AC) specifies the input differential voltage I Vtr – Vcp I required for switching, where Vtr is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and Vcp is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to VIH (AC) – VIL (AC).
2. The typical value of Vix (AC) is expected to be about 0.5 x VDDQ of the transmitting devices and Vix (AC) is expected to track variations in VDDQ.

OCD Default Characteristics

Description	Min	Nom	Max	Unit	Notes
Output Impedance	12.6	18	23.4	Ohms	1, 2
Pull-Up and Pull-Down mismatch	0	-	4	Ohms	1, 2, 3
Output slew rate	1.5	-	4.5	V/ns	1, 4, 5

Notes:

1. Absolute specifications: 0°C ≤ Tcase ≤ 85°C; VDD = 1.8V +/- 0.1V, VDDQ = 1.8V +/- 0.1V.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

Symbol	Parameter	PC2-3200		PC2-4200		PC2-5300		PC2-6400		Units
		min	max	min	max	min	max	min	max	
tAC	DQ output access time from CK/CK	-600	+600	-500	+500	-450	+450	- 400	400	ps
tDQSCK	DQS output access time from CK/CK	-500	+500	-450	+450	-400	+400	- 350	350	ps
tCH	CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tHP	CK half period	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ps
tCK	Clock cycle time, CL=x	5000	8000	3750	8000	3000	8000	2500	8000	ps
tDH(base)	DQ and DM input hold time	275	x	225	x	175	x	125	x	ps
tDS(base)	DQ and DM input setup time	150	x	100	x	100	x	50	x	ps
tIPW	Control & Address input pulse width for each input	0.6	x	0.6	x	0.6	x	0.6	x	tCK
tDIPW	DQ and DM input pulse width for each input	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tHZ	Data-out high-impedance time from CK/CK	x	tAC max	x	tAC max	x	tAC max	x	tAC max	ps
tLZ(DQS)	DQS low-impedance time from CK/CK	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
tLZ(DQ)	DQ low-impedance time from CK/CK	2*tACmin	tAC max	2*tACmin	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	ps
tDQSQ	DQS-DQ skew for DQS and associated DQ signals	x	350	x	300	x	240	x	200	ps
tQHS	DQ hold skew factor	x	450	x	400	x	340	x	300	ps
tQH	DQ/DQS output hold time from DQS	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps
tDQSS	First DQS latching transition to associated clock edge	-0.25	0.25	-0.25	0.25	-0.25	0.25	- 0.25	0.25	tCK
tDQSH	DQS input high pulse width	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tDQSL	DQS input low pulse width	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tDSS	DQS falling edge to CK setup time	0.2	x	0.2	x	0.2	x	0.2	x	tCK
tDSH	DQS falling edge hold time from CK	0.2	x	0.2	x	0.2	x	0.2	x	tCK
tMRD	Mode register set command cycle time	2	x	2	x	2	x	2	x	tCK
tWPST	Write postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tWPRE	Write preamble	0.35	x	0.35	x	0.35	x	0.35	x	tCK
tIH(base)	Address and control input hold time	475	x	375	x	275	x	250	x	ps
tIS(base)	Address and control input setup time	350	x	250	x	200	x	175	x	ps
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tRRD	Active to active command period for 1kb page size products	7.5	x	7.5	x	7.5	x	7.5	x	ns
tRRD	Active to active command period for 2kb page size products	10	x	10	x	10	x	10	x	ns
tFAW	Four Bank Activate period for 1kb page size products	37.5		37.5		37.5		35		ns
tFAW	Four Bank Activate period for 2kb page size products	50		50		50		45		ns
tCCD	CAS to CAS command delay	2		2		2		2	x	tCK
tWR	Write recovery time	15	x	15	x	15	x	15	x	ns

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

AC CHARACTERISTICS

Symbol	Parameter		PC2-3200		PC2-4200		PC2-5300		PC2-6400		Units
			min	max	min	max	min	max	min	max	
tRC	Active to Active/Auto-Refresh command period	CL = 3	55	-	-	-	-	-	-	-	ns
		CL = 4	-		60		-		-		
		CL = 5	-		-		60		57.5		
		CL = 6	-		-		-		60		
tRFC	Auto-Refresh to Active/Auto-Refresh command period	256Mb, 512Mb	105	70000	105	70000	105	70000	105	70000	ns
		1Gb	127.5		127.5		127.5		127.5		
		2Gb	195		195		195		195		
tRCD	Active to Read or Write (with and without Auto-Precharge) delay	CL = 3	15	-	-	-	-	-	-	-	ns
		CL = 4	-		15		-		-		
		CL = 5	-		-		15		12.5		
		CL = 6	-		-		-		15		
tRP	Precharge command period	CL = 3	15	-	-	-	-	-	-	-	ns
		CL = 4	-		15		-		-		
		CL = 5	-		-		15		12.5		
		CL = 6	-		-		-		15		
tRAS	Active to Precharge command	CL = 3	40	70000	-	70000	-	70000	-	70000	ns
		CL = 4	-		45		-		-		
		CL = 5	-		-		45		45		
		CL = 6	-		-		-		45		
tDAL	Auto precharge write recovery + precharge time		WR+tRP	x	WR+tRP	x	WR+tRP	x	WR+tRP	x	tCK
tWTR	Internal write to read command delay		10	x	7.5	x	7.5	x	7.5		ns
tRTP	Internal read to precharge command delay		7.5		7.5		7.5		7.5		ns
tXSNR	Exit self refresh to a non-read command		tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns
tXSRD	Exit self refresh to a read command		200		200		200		200	x	tCK
tXP	Exit precharge power down to any non-read command		2	x	2	x	2	x	2	x	tCK
tXARD	Exit active power down to read command		2	x	2	x	2	x	2	x	tCK
tXARDS	Exit active power down to read command (slow exit, lower power)		6 - AL		6 - AL		7 - AL		8 - AL		tCK
tCKE	CKE minimum pulse width (high and low pulse width)		3		3		3		3		tCK
tAOND	ODT turn-on delay		2	2	2	2	2	2	2	2	tCK
tAON	ODT turn-on		tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +0.7	tAC(min)	tAC(max) + 0.7	ns
tAONPD	ODT turn-on(Power-Down mode)		tAC(min)+ 2	2tCK+tAC (max)+1	tAC(min)+ 2	2tCK+tAC (max)+1	tAC(min)+ 2	2tCK+tAC (max)+1	tAC(min)+ 2	2tCK+tAC (max)+1	ns
tAOFD	ODT turn-off delay		2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK
tAOF	ODT turn-off		tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns
tAOFPD	ODT turn-off (Power-Down mode)		tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK + tAC(max) +1	ns
tANPD	ODT to power down entry latency		3		3		3		3		tCK
tAXPD	ODT power down exit latency		8		8		8		8		tCK
tOIT	OCD drive mode output delay		0	12	0	12	0	12	0	12	ns
tDelay	Minimum time clocks remain ON after CKE asynchronously drops LOW		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns

REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	April 19, 2007	Initial release. Combined PS5EUXX7218XBX and PS5EU6418XBX, add single rank 1Gbit, add 800MHz.	Brian Ouellette Ken Ishiguro
B	October 5, 2007	Add 1Gb PC2-6400 CL5, update all PC2-6400 IDD values	Brian Ouellette
C	June 30, 2008	Add 1R 2Gb configurations	Brian Ouellette
D	April 29, 2009	Add 1Gb 1066 configurations	Brian Ouellette
D1	November 21, 2011	Add new logo and company name. Removed preliminary mark on PN's	
E	November 11 , 2015	Revise 1Gbit based IDD values	

STATEMENT OF COMPLIANCE

Viking Technology(tm), Sanmina-SCI Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.