

MODULE CONFIGURATIONS

Viking Part Number	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR5EU646418EBP	512MB	64Mx64	64M x 8 (8)	FBGA	1	PC2-3200	CL3 (3-3-3)
VR5EU646418EBS	512MB	64Mx64	64M x 8 (8)	FBGA	1	PC2-4200	CL4 (4-4-4)
VR5EU646418EBW	512MB	64Mx64	64M x 8 (8)	FBGA	1	PC2-5300	CL5 (5-5-5)
VR5EU286418EBP	1GB	128Mx64	64M x 8 (16)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU286418EBS	1GB	128Mx64	64M x 8 (16)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU286418EBW	1GB	128Mx64	64M x 8 (16)	FBGA	2	PC2-5300	CL5 (5-5-5)
VR5EU566418FBP	2GB	256Mx64	128M x 8 (16)	FBGA	2	PC2-3200	CL3 (3-3-3)
VR5EU566418FBS	2GB	256Mx64	128M x 8 (16)	FBGA	2	PC2-4200	CL4 (4-4-4)
VR5EU566418FBW	2GB	256Mx64	128M x 8 (16)	FBGA	2	PC2-5300	CL5 (5-5-5)

Features

- 240 pin Unbuffered DIMM
- Single 1.8V ± 0.1V Power Supply
- Burst Length (4, 8)
- Burst type (Sequential & Interleave)
- Auto & Self-Refresh.
- 8k/64ms Refresh Period.
- Differential CLK (#CLK) input.
- On-die termination (ODT)
- Off-chip driver (OCD) impedance calibration
- Serial Presence Detect with EEPROM.
- Lead Free Product.

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PIN CONFIGURATIONS

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VREF	121	VSS	31	DQ19	151	VSS	61	A4	181	VDDQ	91	VSS	211	DM5
2	VSS	122	DQ4	32	VSS	152	DQ28	62	VDDQ	182	A3	92	/DQS5	212	*/DQS14
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	VSS
4	DQ1	124	VSS	34	DQ25	154	VSS	64	VDD	184	VDD	94	VSS	214	DQ46
5	VSS	125	DM0	35	VSS	155	DM3	65	VSS	185	CK0	95	DQ42	215	DQ47
6	/DQS0	126	*/DQS9	36	/DQS3	156	*/DQS12	66	VSS	186	/CK0	96	DQ43	216	VSS
7	DQS0	127	VSS	37	DQS3	157	VSS	67	VDD	187	VDD	97	VSS	217	DQ52
8	VSS	128	DQ6	38	VSS	158	DQ30	68	*PAR IN	188	A0	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	69	VDD	189	VDD	99	DQ49	219	VSS
10	DQ3	130	VSS	40	DQ27	160	VSS	70	A10/AP	190	BA1	100	VSS	220	CK2
11	VSS	131	DQ12	41	VSS	161	*CB4	71	BA0	191	VDDQ	101	SA2	221	/CK2
12	DQ8	132	DQ13	42	*CB0	162	*CB5	72	VDDQ	192	/RAS	102	NC	222	VSS
13	DQ9	133	VSS	43	*CB1	163	VSS	73	/WE	193	/S0	103	VSS	223	DM6
14	VSS	134	DM1	44	VSS	164	*DM8	74	/CAS	194	VDDQ	104	/DQS6	224	*/DQS15
15	/DQS1	135	*/DQS10	45	*/DQS8	165	*/DQS17	75	VDDQ	195	ODT0	105	DQS6	225	VSS
16	DQS1	136	VSS	46	*DQS8	166	VSS	76	**/S1	196	A13	106	VSS	226	DQ54
17	VSS	137	CK1	47	VSS	167	*CB6	77	**ODT1	197	VDD	107	DQ50	227	DQ55
18	*/RESET	138	/CK1	48	*CB2	168	*CB7	78	VDDQ	198	VSS	108	DQ51	228	VSS
19	NC	139	VSS	49	*CB3	169	VSS	79	VSS	199	DQ36	109	VSS	229	DQ60
20	VSS	140	DQ14	50	VSS	170	VDDQ	80	DQ32	200	DQ37	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	VDDQ	171	**CKE1	81	DQ33	201	VSS	111	DQ57	231	VSS
22	DQ11	142	VSS	52	CKE0	172	VDD	82	VSS	202	DM4	112	VSS	232	DM7
23	VSS	143	DQ20	53	VDD	173	*A15	83	/DQS4	203	*/DQS13	113	/DQS7	233	*/DQS16
24	DQ16	144	DQ21	54	BA2	174	*A14	84	DQS4	204	VSS	114	DQS7	234	VSS
25	DQ17	145	VSS	55	*ERR_OUT	175	VDDQ	85	VSS	205	DQ38	115	VSS	235	DQ62
26	VSS	146	DM2	56	VDDQ	176	A12	86	DQ34	206	DQ39	116	DQ58	236	DQ63
27	/DQS2	147	*/DQS11	57	A11	177	A9	87	DQ35	207	VSS	117	DQ59	237	VSS
28	DQS2	148	VSS	58	A7	178	VDD	88	VSS	208	DQ44	118	VSS	238	VDDSPD
29	VSS	149	DQ22	59	VDD	179	A8	89	DQ40	209	DQ45	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	90	DQ41	210	VSS	120	SCL	240	SA1

*Pins are not used in this module
** Pins are used for 2 rank modules



PIN FUNCTION DESCRIPTION

SYMBOL	TYPE	POLARITY	DESCRIPTION
CK0, CK1 /CK0, /CK1	IN	Positive Edge Negative Edge	Clock: CK and /CK are differential clock inputs. All addresses and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output data (DQs, DQS and /DQS) is referenced to the crossings of CK and /CK.
CKE0 ~ CKE1	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
/S0 ~ /S1	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both S[0:1] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state.
ODT0 ~ ODT1	IN	Active High	On-Die Termination control signals
/RAS, /CAS, /WE	IN	Active Low	CAS, WE When sampled at the positive rising edge of the clock, /CAS, /RAS, and /WE define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL18 inputs
VDD	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA [1:0]	IN	-	Selects which SDRAM bank of four or eight is activated.
A [13:0]	IN	-	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, and BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ [63:0]	I/O	-	Data Input/Output pins
DM [7:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
VDD, GND	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
DQS [7:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
/DQS [7:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
/EVENT	Out	-	The optional EVENT pin is reserved for use to flag critical module temperatures and is used in conjunction with a SPD temperature sensing option.
SA [1:0]	IN	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDDSPD on the system planar to act as a pull-up.
VDDSPD	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector, which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operations.

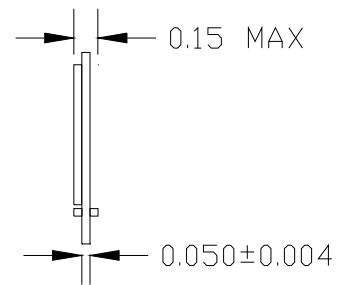
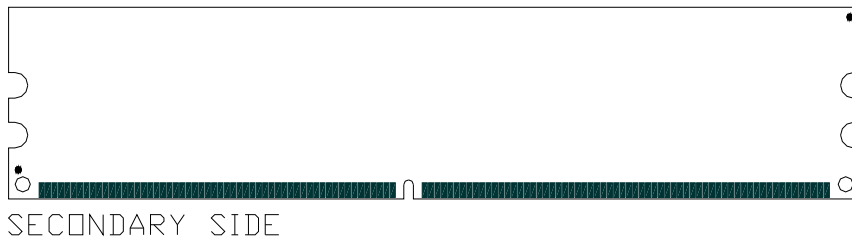
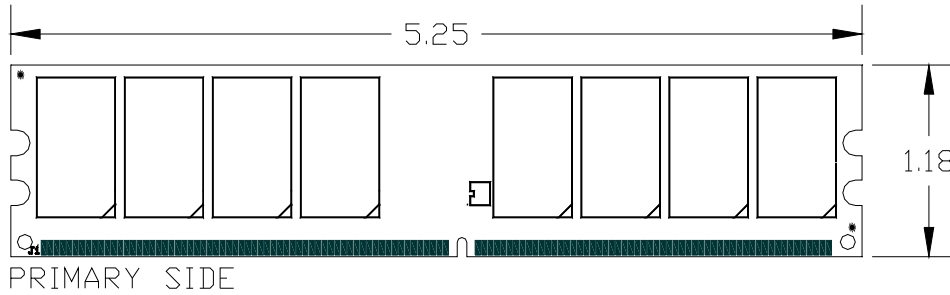
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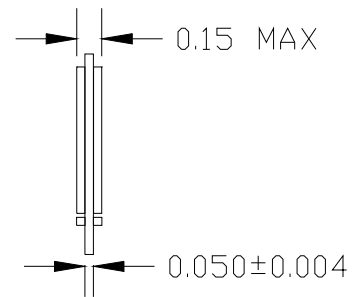
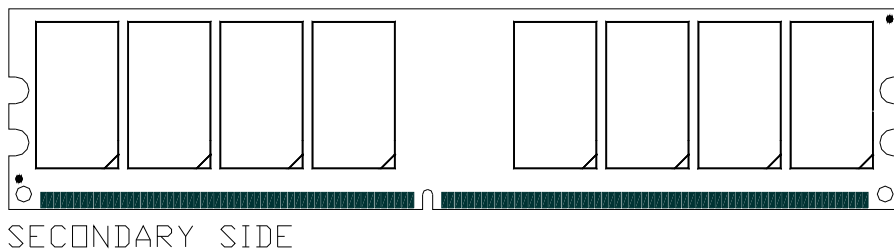
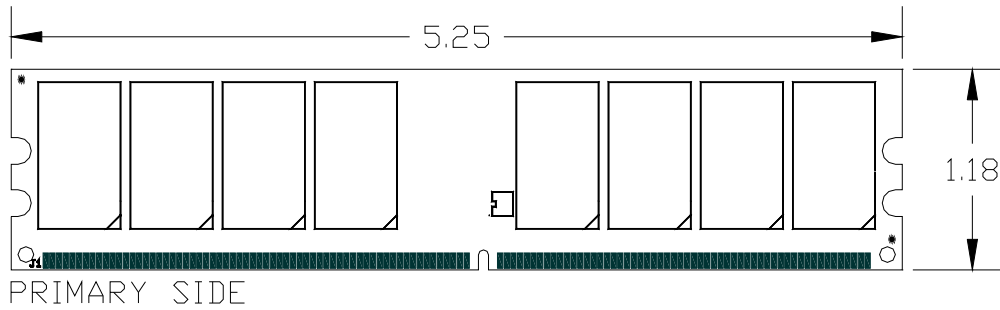
MECHANICAL OUTLINE SINGLE RANK

All dimensions are in inches with a tolerance of +/- 0.005 unless otherwise specified.

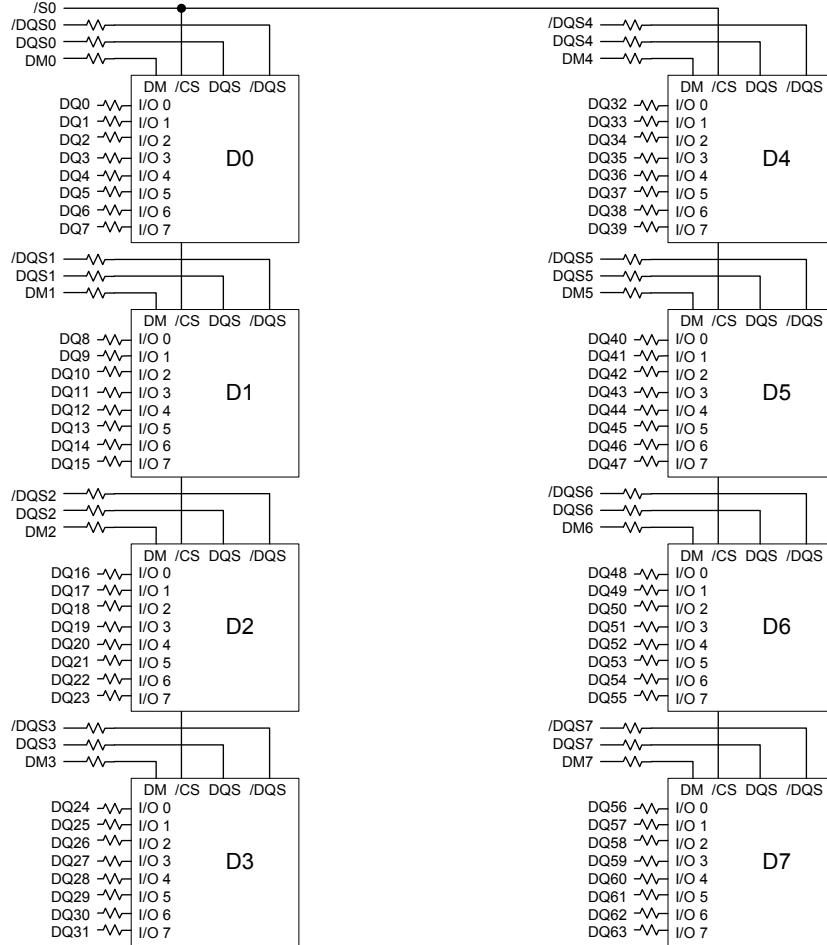


MECHANICAL OUTLINE DUAL RANK

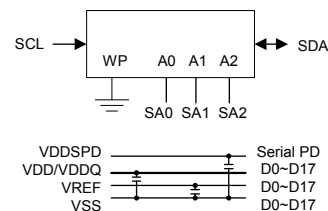
All dimensions are in inches with a tolerance of +/- 0.005 unless otherwise specified.



FUNCTIONAL BLOCK DIAGRAM SINGLE RANK



- BA0-BA2 → BA0-BA2: SDRAMs D0-D7
- A0-An → A0-An: SDRAMs D0-D7
- CKE0 → CKE0: SDRAMs D0-D7
- /RAS → /RAS: SDRAMs D0-D7
- /CAS → /CAS: SDRAMs D0-D7
- /WE → /WE: SDRAMs D0-D7
- ODT0 → ODT0: SDRAMs D0-D7



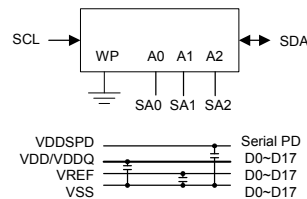
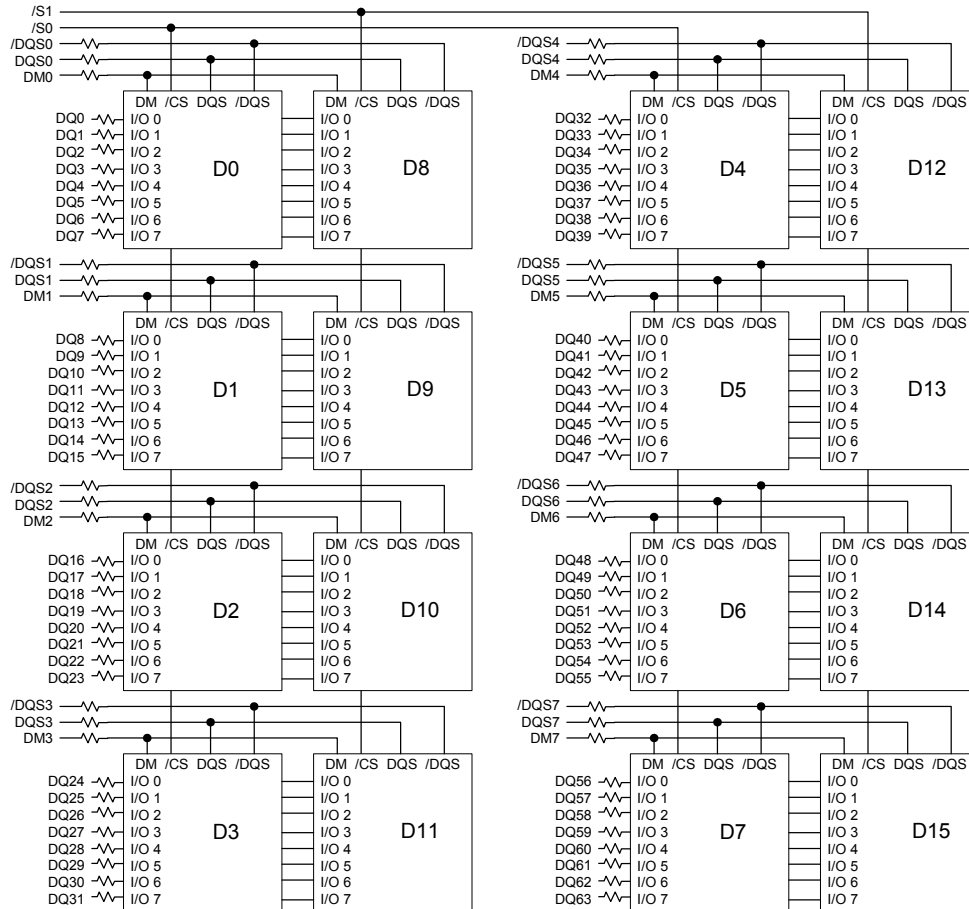
Notes:
1. Unless otherwise noted, resistor values are 22 Ohms +/- 5%

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FUNCTIONAL BLOCK DIAGRAM DUAL RANK



- BA0-BA2 → BA0-BA2: SDRAMs D0-D15
- A0-An → A0-An: SDRAMs D0-D15
- CKE0 → CKE0: SDRAMs D0-D7
- CKE1 → CKE1: SDRAMs D8-D15
- /RAS → /RAS: SDRAMs D0-D15
- /CAS → /CAS: SDRAMs D0-D15
- /WE → /WE: SDRAMs D0-D15
- ODT0 → ODT0: SDRAMs D0-D7
- ODT1 → ODT1: SDRAMs D8-D15

Notes:
1. Unless otherwise noted, resistor values are 22 Ohms +/- 5%

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND	Vin, Vout	-0.5 ~ 2.3	V
Voltage on VDD supply relative to GND	VDD	-1.0 ~ 2.3	V
Voltage on VDDQ supply relative to GND	VDDQ	-0.5 ~ 2.3	V
Storage temperature	TSTG	-55 ~ +100	°C

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_1.8)

Recommended operating conditions (Voltages referenced to GND, Tcase = 0 to 85°C)

Parameter	Symbol	Min.	Max.	Unit	Notes	
Case Temperature	Tcase	0	85	°C		
Supply voltage	VDD	1.7	1.9	V		
Supply voltage for DQ, DQS	VDDQ	1.7	1.9	V		
Input reference voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	1, 2	
EEPROM Supply Voltage	VDDSPD	1.7	3.6	V		
Input high voltage	VIH	VREF + 0.125	VDDQ + 0.3	V		
Input low voltage	VIL	-0.3	VREF - 0.125	V		
Input leakage current	Single Rank	IIL	-40	40	µA	3
Output leakage current	Single Rank	IOL	-5	5	µA	4
Input leakage current	Dual Rank	IIL	-80	80	µA	3
Output leakage current	Dual Rank	IOL	-10	10	µA	4

- Note:**
1. Peak to peak AC noise on VREF may not exceed +/- 2% VREF (DC). VREF is also expected to track noise variation in VDD.
 2. For any pin under test input of 0 V ≤ VIN ≤ VDDQ + 0.3 V.
 3. Any input 0V ≤ Vin ≤ VDD; all other pins not under test = 0V.
 4. 0V ≤ VOUT ≤ VDDQ; DQ and ODT disabled

CAPACITANCE (VDD = 1.8V, TA = 25°C)

Parameter	Symbol	Min		Max		Unit	
		Single Rank	Dual Rank	Single Rank	Dual Rank		
Input capacitance (A0 ~ An, BA0 ~ BA1)	CIN1	13	21	21	37	pF	
Input capacitance (/RAS, /CAS, /WE)	CIN2	13	21	21	37	pF	
Input capacitance (CKE0 ~ *CKE1)	CIN3	13		21		pF	
Input capacitance (/S0 ~*/S1)	CIN4	13		21		pF	
Input capacitance (CK0, /CK0 ~ CK1, /CK1)	CIN5a	8	11	11	17	pF	
Input capacitance (DQS0 ~ DQS7, /DQS0 ~ /DQS7), (DM0 ~ DM7)	400MHz, 533MHz	CIN6a	7.5	10	9	13	pF
	667MHz	CIN6c	7.5	10	8.5	12.5	pF
Data input/output capacitance (DQ0 ~ DQ63)	400MHz, 533MHz	COUta	7.5	10	9	13	pF
	667MHz	COUtc	7.5	10	8.5	12.5	pF

*Used in dual ranked module only

DC CHARACTERISTICS DEFINITIONS (Recommended operating conditions unless otherwise noted, Tcase = 0 to 85 °C)

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Note: 1. Calculated values are from component data. ODT disabled. IDD1, TDD4R are defined with the outputs disabled.

Parameter	Symbol	Test Condition	Unit	Note	
Operating one bank active-precharge current	IDD0	tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2	
Operating one bank active-read-precharge current	IDD1	IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2	
Precharge power-down current	IDD2P	All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3	
Precharge quiet standby current	IDD2Q	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3	
Precharge standby current	IDD2N	All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3	
Active power-down current	IDD3P-F	All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MR(12) = 0	mA	1, 3
	IDD3P-S		Slow PDN Exit MR(12) = 1		
Active standby current	IDD3N	All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3	
Operating burst read current	IDD4R	All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2	
Operating burst write current	IDD4W	All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2	
Auto refresh current	IDD5	tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3	
Self refresh current	IDD6	CK and /CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	mA	1, 3	
Operating bank interleave read current	IDD7	All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R	mA	1, 2	

2. For dual rank modules the other rank is in IDD2P Precharge Power-Down Standby Current mode.
3. For dual rank modules both ranks are in the same IDD current mode.

DC CHARACTERISTICS CURRENTS SINGLE RANK 512Mb

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Symbol	VR5EU646418EBP PC2-3200 CL3 (3-3-3)	VR5EU646418EBS PC2-4200 CL4 (4-4-4)	VR5EU646418EBW PC2-5300 CL5 (5-5-5)	Unit
IDD0	640	640	680	mA
IDD1	760	760	800	mA
IDD2P	64	64	64	mA
IDD2Q	240	240	280	mA
IDD2N	280	280	320	mA
IDD3P-F	240	240	240	mA
IDD3P-S	96	96	96	mA
IDD3N	400	400	440	mA
IDD4R	880	1000	1160	mA
IDD4W	880	960	1120	mA
IDD5	1120	1120	1200	mA
IDD6	64	64	64	mA
IDD7	1760	1760	1760	mA

DC CHARACTERISTICS CURRENTS DUAL RANK 512Mb

Symbol	VR5EU286418EBP PC2-3200 CL3 (3-3-3)	VR5EU286418EBS PC2-4200 CL4 (4-4-4)	VR5EU286418EBW PC2-5300 CL5 (5-5-5)	Unit
IDD0	704	704	744	mA
IDD1	824	824	864	mA
IDD2P	128	128	128	mA
IDD2Q	480	480	560	mA
IDD2N	560	560	640	mA
IDD3P-F	480	480	480	mA
IDD3P-S	192	192	192	mA
IDD3N	800	800	880	mA
IDD4R	944	1064	1224	mA
IDD4W	944	1024	1184	mA
IDD5	2240	2240	2400	mA
IDD6	128	128	128	mA
IDD7	1824	1824	1824	mA

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DC CHARACTERISTICS CURRENTS DUAL RANK 1Gb

Symbol	VR5EU566418FBP PC2-3200 CL3 (3-3-3)	VR5EU566418FBS PC2-4200 CL4 (4-4-4)	VR5EU566418FBW PC2-5300 CL5 (5-5-5)	Unit
IDD0	800	800	840	mA
IDD1	880	880	920	mA
IDD2P	240	240	240	mA
IDD2Q	640	720	720	mA
IDD2N	640	720	720	mA
IDD3P-F	560	560	640	mA
IDD3P-S	288	288	288	mA
IDD3N	880	960	960	mA
IDD4R	1040	1160	1360	mA
IDD4W	1040	1160	1360	mA
IDD5	3360	3440	3520	mA
IDD6	240	240	240	mA
IDD7	2200	2360	2520	mA

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AC INPUT TEST CONDITIONS

Parameter	Symbol	Value	Unit	Notes
Input reference voltage	VREF	0.50 * VDDQ	V	
Input signal maximum peak to peak swing	VSWING _(MAX)	1.0	V	
Input signal maximum slew rate	SLEW	1.0	V/ns	1, 2

Notes:

1. The Input signal minimum slew rate is to be maintain over the range from VIL(DC) max to VIL(AC) min for raising edges and the range from VIH(DC) min to VIL(AC) max for falling edges.
2. AC timings are reference with input waveforms switching from VIL(AC) to VIH(AC) on the positive transition and VIH(AC) to VIL(AC) on the negative transitions.

AC OPERATING CONDITIONS (VDD = 1.8V ± 0.1V, TOPR = 0 to 85 °C)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Input Differential Voltage	VID(ac)	0.5	VDDQ +0.6	V	1
Input Crossing Point Voltage	VIX(ac)	0.5*VDDQ -0.175	0.5*VDDQ +0.175	V	2

Notes:

1. VID (AC) specifies the input differential voltage $|V_{tr} - V_{cp}|$ required for switching, where V_{tr} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{cp} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to VIH (AC) – VIL (AC).
2. The typical value of Vix (AC) is expected to be about 0.5 x VDDQ of the transmitting devices and Vix (AC) is expected to track variations in VDDQ.

OCD Default Characteristics

Description	Min	Nom	Max	Unit	Notes
Output Impedance	12.6	18	23.4	Ohms	1, 2
Pull-Up and Pull-Down mismatch	0	-	4	Ohms	1, 2, 3
Output slew rate	1.5	-	4.5	V/ns	1, 4, 5

Notes:

1. Absolute specifications: 0°C ≤ Tcase ≤ 85°C; VDD = 1.8V +/- 0.1V, VDDQ = 1.8V +/- 0.1V.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Symbol	Parameter	DDR2-400		DDR2-533		DDR2-667		Unit	
		min	max	min	max	min	max		
tAC	DQ output access time from CK / CK	- 600	+ 600	-500	+500	-450	+450	ps	
tDQSCK	DQS output access time from CK / CK	- 500	+ 500	-450	+450	-400	+400	ps	
tCH	CK, CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCL	CK, CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tHP	Clock half period	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)			
tCK	Clock cycle time	CL = 3	5000	8000	5000	8000	5000	8000	ps
		CL = 4	5000	8000	3750	8000	3000	8000	ps
		CL = 5	N/A	N/A	3750	8000	3000	8000	ps
tIS	Address and control input setup time	350 (base)	-	250 (base)	-	200 (base)	-	ps	
tIH	Address and control input hold time	475 (base)	-	375 (base)	-	275 (base)	-	ps	
tDH	DQ and DM input hold time	150 (base)	-	100 (base)	-	150 (base)	-	ps	
tDS	DQ and DM input setup time	275 (base)	-	225 (base)	-	175 (base)	-	ps	
tIPW	Address and control input pulse width (each input)	0.6	-	0.6	-	0.6	-	tCK	
tDIPW	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	tCK	
tHZ	Data-out high-impedance time from CK / CK	-	tACmax	-	tACmax	-	tACmax	ps	
tLZ(DQS)	Data-out low-impedance time from CK / CK	tACmin	tACmax	tACmin	tACmax	tACmin	tACmax	ps	
tLZ(DQ)	Data-out low-impedance time from CK / CK	2*tACmin	2*tACmax	2*tACmin	2*tACmax	2*tACmin	2*tACmax	ps	
tDQSQ	DQS-DQ skew (for DQS & associated DQ signals)	-	350	-	300	-	240	ps	
tQHS	Data hold skew factor	-	450	-	400	-	340	ps	
tQH	Data output hold time from DQS	tHP-tQHS	-	tHP-tQHS	-	tHP-tQHS	-		
tDQSS	Write command to 1st DQS latching transition	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	tCK	
tDQSL	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	0.35	-	tCK	
tDQSH	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	0.35	-	tCK	
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	tCK	
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	tCK	
tMRD	Mode register set command cycle time	2	-	2	-	2	-	tCK	
tWPRES	Write preamble setup time	0	-	0	-	0	-	ps	
tWPRE	Write preamble	0.25	-	0.25	-	0.35	-	tCK	
tWPST	Write postamble	0.40	0.60	0.40	0.60	0.40	0.60	tCK	
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
tRPST	Read postamble	0.40	0.60	0.40	0.60	0.40	0.60	tCK	
tRAS	Active to Precharge command	CL = 3	40	70000	N/A	N/A	N/A	N/A	ns
		CL = 4	40	70000	40	70000	39	70000	ns
		CL = 5	N/A	N/A	39	70000	39	70000	ns

Viking Technology ♦ 20091 Ellipse ♦ Foothill Ranch, CA 92610
Tel (800) 338-2361 Fax (949) 666-8159 ♦ Website: <http://www.vikingtechnology.com>

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AC CHARACTERISTICS

Symbol	Parameter		DDR2-400		DDR2-533		DDR2-667		Unit
			min	max	min	max	min	max	
tRC	Active to Active/Auto-Refresh command period	CL = 3	55	-	N/A	N/A	N/A	N/A	ns
		CL = 4	55	-	55	-	51	-	ns
		CL = 5	N/A	N/A	55	-	54	-	ns
tRFC	Auto-Refresh to Active/Auto-Refresh command period	256Mb, 512Mb	105	70000	105	70000	105	70000	ns
		1Gb	127.5		127.5				
tRCD	Active to Read or Write (with and without Auto-Precharge) delay	CL = 3	15	-	N/A	N/A	N/A	N/A	ns
		CL = 4	15	-	15	-	12	-	ns
		CL = 5	N/A	N/A	15	-	12	-	ns
tRP	Precharge command period	CL = 3	15	-	N/A	N/A	N/A	N/A	ns
		CL = 4	15	-	15	-	12	-	ns
		CL = 5	N/A	N/A	15	-	12	-	ns
tRRD	Active bank A to Active bank B command period	x8 (1k page size)	7.5	-	7.5	-	7.5	-	ns
tCCD	CAS A to CAS B command period		2		2		2		tCK
tWR	Write recovery time		15	-	15	-	12	-	ns
tDAL	Auto-Precharge write recovery + precharge time		WR+tRP	-	WR+tRP	-	WR+tRP	-	tCK
tWTR	Internal Write to Read command delay		10	-	7.5	-	7.5	-	ns
tRTP	Internal Read to Precharge command delay		7.5	-	7.5	-	7.5	-	ns
tXARD	Exit power down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	tCK
tXARDS	Exit active power-down mode to Read command (slow exit, lower power)		6 - AL	-	6 - AL	-	7 - AL	-	tCK
tXP	Exit precharge power-down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	tCK
tXSRD	Exit Self-Refresh to Read command		200	-	200	-	200	-	tCK
tXSNR	Exit Self-Refresh to non-Read command		tRFC+10	-	tRFC+10		tRFC+10	-	ns
tCKE	CKE minimum high and low pulse width		3	-	3	-	3	-	tCK
tREFI	Average periodic refresh Interval		-	7.8	-	7.8	-	7.8	µs
tOIT	OCD drive mode output delay		0	12	0	12	0	12	ns
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW		tIS+tCK+tIH	-	tIS+tCK+tIH	-	tIS+tCK+tIH	-	ns

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REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	February 7, 2006	Initial release	Brian Ouellette
A1	July 30, 2012	Add new logo and company name	

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