DDR3/DDR3L
ECC LRDIMM
1.5V/1.35V

The Viking Load Reduced DIMM (LRDIMM) provides a DDR3 JEDEC standard interface that is fully buffered to provide a single load per signal, per module. The buffer reduces the capacitive loading on the memory channel address, control, DQ and DQS nodes to enable large memory capacities at high memory bandwidths. This version of the LRDIMM is a planer, 52mm tall DIMM.

REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	5/06/13	Preliminary based on 1440 PCB	
A1	11/16/13	Deleted 1333 support. Added product photo	
A2	11/24/13	Revised max thickness to include IMB. Revised notes for DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_1.5). Removed preliminary watermark	IDC/ Brian Ouellette
A3	1/2/14	Updated datasheet format	
B	7/20/17	Updated datasheet format	

Legal Information

Legal Information

STATEMENT OF COMPLIANCE

Viking Technology, Sanmina Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.

All printed circuit boards (PCBs) have a flammability rating of UL94V-0.

Ordering Information and Module Configuration

Viking Part Number	Voltage	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR7EL2G7258GBZ	1.5V	16GB	2Gx72	256Mx8 (72)	BGA	8	PC3-6400	CL6 (6-6-6)
VR7EL2G7258GBA	1.5V	16GB	2Gx72	256Mx8 (72)	BGA	8	PC3-8500	CL7 (7-7-7)
VR7EL4G7258HBZ	1.5V	32GB	4Gx72	512Mx8 (72)	BGA	8	PC3-6400	CL6 (6-6-6)
VR7EL4G7258HBA	1.5V	32GB	4Gx72	512Mx8 (72)	BGA	8	PC3-8500	CL7 (7-7-7)
VR7EL2G7298GBZ	1.35V	16GB	2Gx72	256Mx8 (72)	BGA	8	PC3-6400	CL6 (6-6-6)
VR7EL2G7298GBA	1.35V	16GB	2Gx72	256Mx8 (72)	BGA	8	PC3-8500	CL7 (7-7-7)
VR7EL4G7298HBZ	1.35V	32GB	4Gx72	512Mx8 (72)	BGA	8	PC3-6400	CL6 (6-6-6)
VR7EL4G7298HBA	1.35V	32GB	4Gx72	512Mx8 (72)	BGA	8	PC3-8500	CL7 (7-7-7)

Features

- JEDEC Standard Power
  - DDR3: VDD = VDDQ = 1.5V ± 5%
  - DDR3L: VDD = VDDQ = 1.35V ± 5%
  - 1.35V Backwards compatible to 1.5V VDD
  - VDDSPD = +3.30V ± 10%
- 240-pin Load-Reduced Dual-In-Line Memory Module with parity bit for address and control bus
- Onboard Integrated Memory Buffer (iMB)
- Multi-rank DIMM with single terminated load on all signals
- Programmable CAS Latency: 6, 7, 8
- Programmable CAS Write Latency (CWL).
- Programmable Additive Latency (Posted CAS)
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity
- Refresh. Self Refresh and Power Down Modes
- ZQ Calibration for output driver and ODT
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.
- Serial Presence Detect with EEPROM
- Two On-DIMM Thermal Sensors
- Asynchronous Reset
- Supports ECC error detection and correction
- LRDIMM dimensions (52 mm)
- RoHS Compliant

Nomenclature

Module Standard	SDRAM Standard	Clock
PC3-6400	DDR3-800	400MHz
PC3 -8500	DDR3-1066	533MHz

Addressing

Parameter	16GB	32GB
Refresh count	8K	8K
Row address	32K A[14:0]	64K A[15:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Column address	1K A[9:0]	1K A[9:0]

PIN CONFIGURATIONS

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VREFDQ	121	VSS	31	DQ25	151	VSS	61	A2	181	A1	91	DQ41	211	VSS
2	VSS	122	DQ4	32	VSS	152	DQS12 **	62	VDD	182	VDD	92	VSS	212	DQS14 **
3	DQ0	123	DQ5	33	DQS3#	153	DQS12# **	63	NC*	183	VDD	93	DQS5#	213	DQS14# **
4	DQ1	124	VSS	34	DQS3	154	VSS	64	NC*	184	CK0	94	DQS5	214	VSS
5	VSS	125	DQS9 **	35	VSS	155	DQ30	65	VDD	185	CK0#	95	VSS	215	DQ46
6	DQS0#	126	DQS9# **	36	DQ26	156	DQ31	66	VDD	186	VDD	96	DQ42	216	DQ47
7	DQS0	127	VSS	37	DQ27	157	VSS	67	VREFCA	187	EVENT#, NC	97	DQ43	217	VSS
8	VSS	128	DQ6	38	VSS	158	CB4	68	Par_In	188	A0	98	VSS	218	DQ52
9	DQ2	129	DQ7	39	CB0	159	CB5	69	VDD	189	VDD	99	DQ48	219	DQ53
10	DQ3	130	VSS	40	CB1	160	VSS	70	A10 / AP	190	BA1	100	DQ49	220	VSS
11	VSS	131	DQ12	41	VSS	161	DQS17 **	71	BA0	191	VDD	101	VSS	221	DQS15 **
12	DQ8	132	DQ13	42	DQS8#	162	DQS17# **	72	VDD	192	RAS#	102	DQS6#	222	DQS15# **
13	DQ9	133	VSS	43	DQS8	163	VSS	73	WE#	193	S0#	103	DQS6	223	VSS
14	VSS	134	DQS10 **	44	VSS	164	CB6	74	CAS#	194	VDD	104	VSS	224	DQ54
15	DQS1#	135	DQS10# **	45	CB2	165	CB7	75	VDD	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	VSS	46	CB3	166	VSS	76	S1#	196	A13	106	DQ51	226	VSS
17	VSS	137	DQ14	47	VSS	167	NC(TEST)	77	ODT1	197	VDD	107	VSS	227	DQ60
18	DQ10	138	DQ15	48	VTT	168	RESET#	78	VDD	198	S3#	108	DQ56	228	DQ61
19	DQ11	139	VSS	**KEY**				79	S2#	199	VSS	109	DQ57	229	VSS
20	VSS	140	DQ20	49	VTT	169	CKE1	80	VSS	200	DQ36	110	VSS	230	DQS16 **
21	DQ16	141	DQ21	50	CKE0	170	VDD	81	DQ32	201	DQ37	111	DQS7#	231	DQS16# **
22	DQ17	142	VSS	51	VDD	171	A15	82	DQ33	202	VSS	112	DQS7	232	VSS
23	VSS	143	DQS11 **	52	BA2	172	A14	83	VSS	203	DQS13 **	113	VSS	233	DQ62
24	DQS2#	144	DQS11# **	53	Err_Out#	173	VDD	84	DQS4#	204	DQS13#**	114	DQ58	234	DQ63
25	DQS2	145	VSS	54	VDD	174	A12 / BC#	85	DQS4	205	VSS	115	DQ59	235	VSS
26	VSS	146	DQ22	55	A11	175	A9	86	VSS	206	DQ38	116	VSS	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	VDD	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	VSS	57	VDD	177	A8	88	DQ35	208	VSS	118	SCL	238	SDA
29	VSS	149	DQ28	58	A5	178	A6	89	VSS	209	DQ44	119	SA2	239	VSS
30	DQ24	150	DQ29	59	A4	179	VDD	90	DQ40	210	DQ45	120	VTT	240	VTT
				60	VDD	180	A3								

Note: All pins functionally the same as a DDR3 RDIMM, except for CK1/CK1# at pins 63 and 64, which are not needed for the LRDIMM.
* NC=No connect
**** Not available for 8 rank DIMMs**

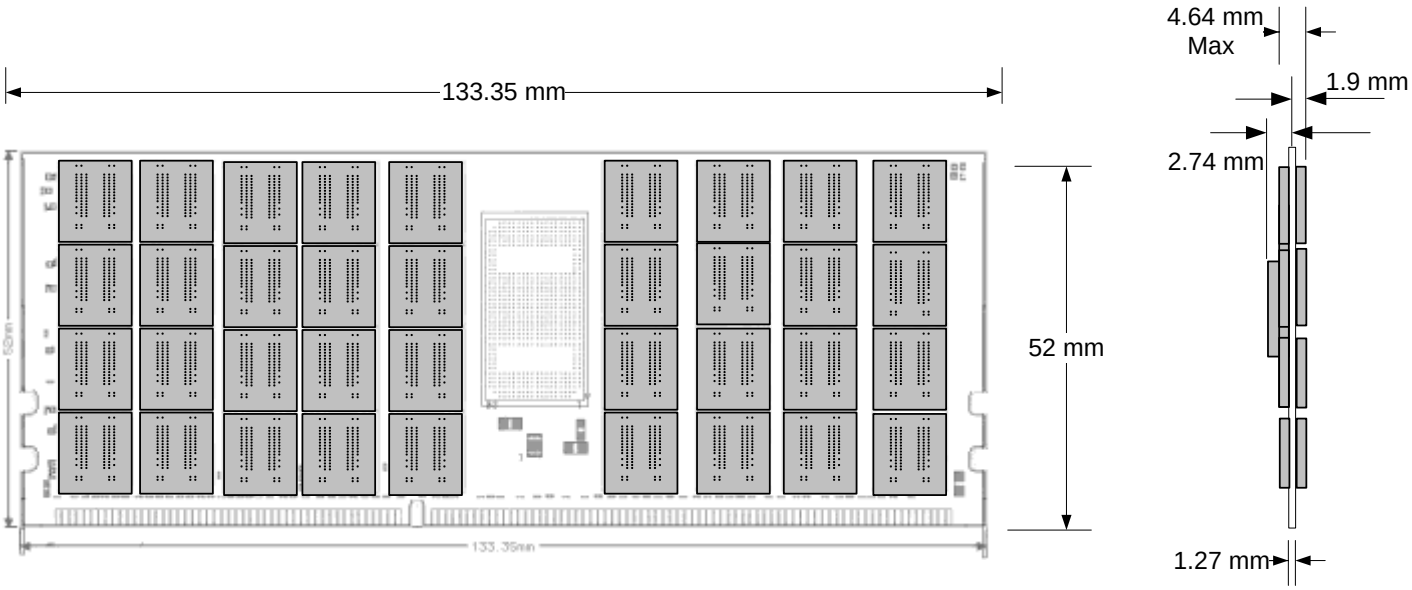
PIN FUNCTION DESCRIPTION

SYMBOL	TYPE	POLARITY	DESCRIPTION
CK0/ CK0#	IN		Differential pair of system clock inputs that drives input to iMB.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[3:0]#	IN	Active Low	Module rank addressing chip selects: Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the memory buffer on the DIMM when both inputs are high. When both S[1:0] are high, all memory buffer outputs (except CKE, ODT and Chip select) remain in the previous state. S[3:2] operate similarly to S[1:0]
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS#, CAS#, WE#	IN	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operation to be executed by the SDRAM.
VREFDQ	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
VREFCA	Supply		Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S1#, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	-	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[15:13, 12/BC,11, 10/AP,9:0]	IN	-	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for ''BL on the fly'' during CAS# command. The address inputs also provide the op-code during Mode Register Set commands.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input/Output pins
VDD, VSS	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
DM [8:0]	IN	Active High	Not available for 8rank DIMMs
VDD, VSS	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
VTT	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[8:0] DQS [8:0]#	I/O		Differential data strobe for input and output data.
DQS[17:9] DQS [17:9]#	I/O		Not available for 8rank DIMMs
SA [2:0]	IN	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDDSPD on the system planar to act as a pullup. (i.e. temperature sensing data)
EVENT#	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT pin on TS/SPD part or iMB
VDDSPD	Supply	-	Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET#	IN		The RESET pin is connected to the RST pin on the memory buffer. When low, all memory buffer outputs will be driven low and the clocks to the DRAMs will be set to low level
Par_In	IN		Parity bit for the Address and Control bus. (“1 “: Odd, “0 “: Even)
Err_Out#	OUT		Parity error found in the Address and Control bus
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)
NC			No Connect, Not used

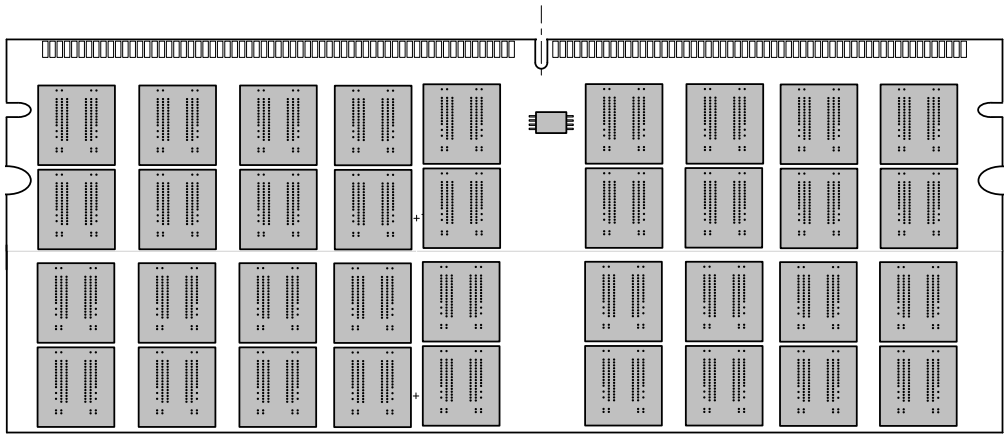
MECHANICAL OUTLINE 8-RANK

Dimensions are in millimeters. (Tolerance is +/- 0.05mm, unless otherwise stated. Nominal DIMM thickness is 4.45mm

SIDE VIEW



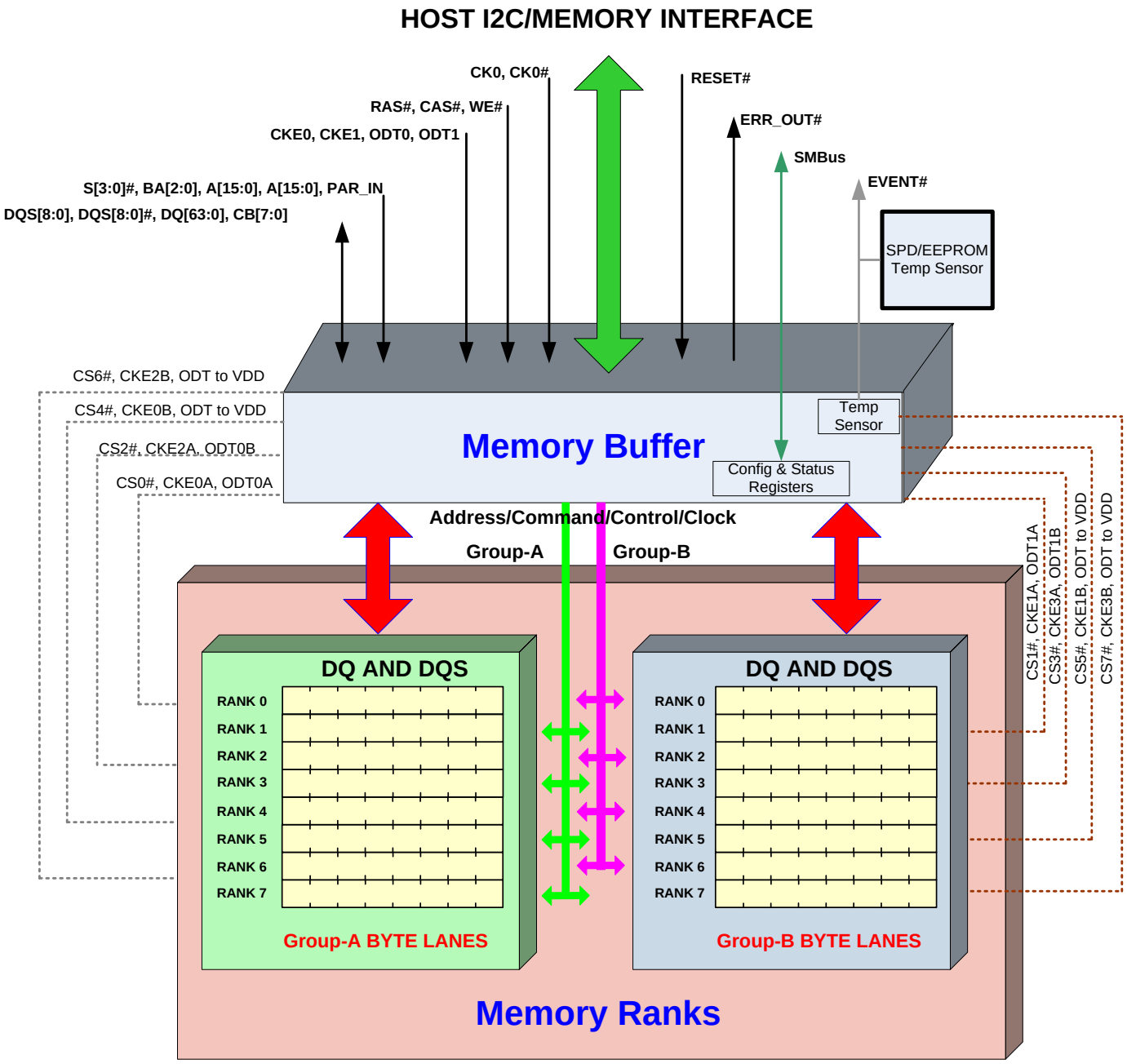
FRONT



BACK

Note: All dimensions in mm

FUNCTIONAL BLOCK DIAGRAM 8-RANK



DQ and DQS MAPPING ON THE HOST SIDE OF iMB

Byte Group	DQ								DQS	
	0	1	2	3	4	5	6	7		
0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQS0	DQS0#
1	DQ8	DQ9	DQ10	DQ11	DQ12	DQ13	DQ14	DQ15	DQS1	DQS1#
2	DQ16	DQ17	DQ18	DQ19	DQ20	DQ21	DQ22	DQ23	DQS2	DQS2#
3	DQ24	DQ25	DQ26	DQ27	DQ28	DQ29	DQ30	DQ31	DQS3	DQS3#
4	DQ32	DQ33	DQ34	DQ35	DQ36	DQ37	DQ38	DQ39	DQS4	DQS4#
5	DQ40	DQ41	DQ42	DQ43	DQ44	DQ45	DQ46	DQ47	DQS5	DQS5#
6	DQ48	DQ49	DQ50	DQ51	DQ52	DQ53	DQ54	DQ55	DQS6	DQS6#
7	DQ56	DQ57	DQ58	DQ59	DQ60	DQ61	DQ62	DQ63	DQS7	DQS7#
8	CB0	CB1	CB2	CB3	CB4	CB5	CB6	CB7	DQS8	DQS8#

OVERVIEW OF LRDIMM MODULE OPERATION

The Load Reduced DIMM (LRDIMM) has the same memory interface as the JEDEC standard DDR3 RDIMM but unlike a DDR3 Register DIMM which only buffers the Command, Address, Control and Clock, the LRDIMM provides additional buffering for the Data (DQ) interface between the Memory Controller and the DRAM components. The onboard Integrated Memory Buffer (iMB) on each LRDIMM enables larger memory capacities at higher memory bandwidths by providing a single load per signal, per module, for all address, control, DQ and DQS nodes and reduces the capacitive loading on the memory channel data bus.

Similar to DDR3 RDIMM's, the clock, control, command, and address buses are routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated. This differs from the tree structure of the DDR2 technology, where the termination is off the module near the connector). Inherent in the fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the same write-leveling feature of DDR3 RDIMM's. The LRDIMM uses a DQS/DQS# differential pair to capture data and CK/CK# differential pair to capture commands, addresses, and control signals. The data strobes and differential clocks ensure noise immunity by providing precise crossing points to capture the input signals.

The iMB on the 8 rank DIMM uses rank multiplication (RM) to decode the four chip select lines S[3:0] into 8 chip enables. The default value for 8 Rank DIMM's is RM =4 although the hardware connections on the 8 rank DIMM support both RM=2 and RM=4 configurations. For 32GB DIMMs, Rank Multiplication (RM) is the default factor of 4. (Note however, for 16GB 8 rank DIMMs, the iMB control word register F0RC15_14 (0Fh) needs an update though the SMBus or through in-band access as well as a BIOS update on the controller side to change the RM factor to 2 (using 2Gb DRAM)).

The iMB supports 8-bank DRAM using a DDR3 8n prefetch architecture which transfers two data words per clock cycle at the I/O pins. A single read or write access for the DRAM module consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

All memory control for the DRAM resides in the host, including memory request initiation, timing, scrubbing and power management. The iMB handles memory requests to and from the local DIMM by using control and status registers that are accessible through the SMBus, as well as through in-band channel commands. These registers can be read by software from the SMBus host any time the memory buffer is powered, except when the memory buffer is in clock-stopped power-down mode, or when the device RESET# pin is asserted There are 3 types of LRDIMM resets:

1) SMBus reset which affect only the SMBus interface.
2) Soft reset generated by setting control word F2RC1, DA3 to '1'.
3) Hard reset when the RESET# signal is low.

RESET# is initiated by the host. It can be asynchronous to the clock including power up or in the middle of DRAM commands. Under these conditions, the iMB will be reset and the contents of DRAM memory are not guaranteed. Upon assertion of RESET#:

- All input receivers are disabled, and can be left floating.
- DRAM CKE and RESET# are driven LOW asynchronously.
- DQ/DQS are don't care. All DRAM C/A inputs (except CKE) are floated.
- DRAM CK/CK# are floated.
- All Configuration and Status Register (CSR) bits are set to their default values.
- All Control Word registers are restored to their default states.
- All internal state machines are put in their default state.
- The "sticky bits" are cleared in the iMB registers that hold the results of the DRAM interface training.

The host can initiate multiple soft resets if needed during LRDIMM initialization and the settings that were established during previous DRAM interface training will not be cleared.

The iMB can accept parity bits from the host memory controller. Even parity is calculated from all cmd and address signals (Note CKE, ODT, and S# are not included in parity). The last bit of the sum is compared to the parity signal provided by the system at the Par_In pin. Parity errors are flagged on the Err_Out# pin and checked during control-word programming.

There are 2 temperature sensors on the LRDIMM. A class-C temperature sensor is located within the memory buffer to monitor the temperature of the iMB and will assert the EVENT# pin if the temperature thresholds are exceeded. This temperature sensor is accessible through the SMBus. The second temperature sensor is a class-B temperature sensor integrated with the SPD EPPROM to monitor the module temperature using a conductive pad under the EEPROM. The EEPROM temperature is converted into a digital word via the SMBus. There are user-programmable registers on the EEPROM to create unique temperature-sensing solutions based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C. All other SPD EEPROM functionally is the same as JEDEC standard DDR3 RDIMM's. The lower 128 bytes of data is programmed to comply with JEDEC standard JC-45 to contain the characteristics of the DIMM and the upper 128 bytes contain vendor specific information.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND		-0.4 ~ 1.975	V
Voltage on VDD supply relative to GND	VDD	-0.4 ~ 1.975	V
Voltage on VDDQ supply relative to GND	VDDQ	-0.4 ~ 1.975	V
Voltage on VDDSPD supply relative to GND	VDDSPD	-0.5 to +6.5	V
Storage temperature	TSTG	-55 ~ +100	°C

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_1.5)

Recommended operating conditions: Voltages referenced to GND, Module Ambient = 0 to 70°C

Parameter	Symbol	Min.	Max.	Unit	Notes
DRAM Case Temperature	DRAM Tcase	0	95	ºC	4
Supply voltage (1.5V ± 5%)	VDD	1.425	1.575	V	1, 2
Supply voltage for DQ, DQS @ 1.5V	VDDQ	1.425	1.575	V	1, 2
Supply voltage (1.35V ± 5%)	VDD	1.283	1.45	V	1, 2
Supply voltage for DQ, DQS @ 1.35V	VDDQ	1.283	1.45	V	1, 2
Reference Voltage for DQ, DM inputs	VREFDQ(DC)	0.49 x VDD	0.51 x VDD	V	3, 5
Reference Voltage for ADD, CMD inputs	VREFCA(DC)	0.49 x VDD	0.51 x VDD	V	3, 4
Termination Reference Current	I_{VTT}	-600	600	mA	
Termination Voltage	VTT	0.49 x VDD	0.51 x VDD	V	3

Parameter	Symbol	Min.	Max.	Unit	Notes
EEPROM Supply Voltage: +3.30V ± 10%	VDDSPD	2.97	3.63	V	
Input high voltage (VDD= 1.5V)	VIH(AC)	VREF + 0.175	-	V	
	VIH(DC)	VREF + 0.100	VDD		
Input low voltage (VDD = 1.5V)	VIL(AC)	-	VREF - 0.175	V	
	VIL(DC)	VSS	VREF – 0.100		
Input high voltage(VDD = 1.35V)	VIH(AC)	VREF + 0.160	-	V	
	VIH(DC)	VREF + 0.090	VDD		
Input low voltage (VDD = 1.35V)	VIL(AC)	-	VREF - 0.160	V	
	VIL(DC)	VSS	VREF – 0.090		

Notes:
1. VDDQ tracks with VDD. VDDQ must be less than or equal to VDD. AC parameters are measured with VDD and VDDQ tied together.
2. The ac peak noise on VREF may not allow VREF to deviate from VREF.DC by more than ±1% VDD (for reference: approx. ± 15 mV).
3. For reference: approx. VDD/2 ± 15 mV.
4. Refresh rate required to be doubled (tREFI = 3.9µs) when 85°C < TC < 95°C
5. DM inputs not available for 8 ranks DIMM's.

iMB SPECIFICATIONS

Symbol	Parameter	Signals	Min	Nom	Max	Unit
	DC Supply voltage = 1.50 **(DDR3)**	VDD, VDDA,VDDP	1.425	1.5	1.575	V
	DC Supply voltage = 1.35 **(DDR3L)**	VDD, VDDA,VDDP	1.283	1.35	1.451	V
VCCSPD	SMBus Interface Supply voltage	VCCSPD	3	3.3	3.6	V
V_{REF}	DC Reference voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
V_{TT}	DC Termination voltage[1]		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
$V_{IH(AC)}$	AC HIGH-level input voltage (DDR3)	CMD/ADD/CTRL inputs[2]	V_{REF} + 0.1	–	V_{DD} + 0.4	V
$V_{IL(AC)}$	AC LOW-level input voltage (DDR3)	CMD/ADD/CTRL inputs	–0.4	–	V_{REF} – 0.1	V
$V_{IH(DC)}$	DC HIGH-level input voltage (DDR3)	CMD/ADD/CTRL inputs	V_{REF} + 0.1	–	V_{DD}	V
$V_{IL(DC)}$	DC LOW-level input voltage (DDR3)	CMD/ADD/CTRL inputs	V_{SS}	–	V_{REF} – 0.1	V
$V_{IH(AC)\_DQ}$	AC HIGH-level input voltage (DDR3)	DQ inputs	V_{REF} + 0.1	–	V_{DD} + 0.4	V
$V_{IL(AC)\_DQ}$	AC LOW-level input voltage (DDR3)	DQ inputs	–0.4	–	V_{REF} – 0.1	V
$V_{IH(DC)\_DQ}$	DC HIGH-level input voltage (DDR3)	DQ inputs	V_{REF} + 0.1	–	V_{DD}	V
$V_{IL(DC)\_DQ}$	DC LOW-level input voltage (DDR3)	DQ inputs	V_{SS}	–	V_{REF} – 0.1	V
$V_{IH(AC)}$	AC HIGH-level input voltage (DDR3L)	CMD/ADD/CTRL inputs	V_{REF} + 0.09	–	V_{DD} + 0.2	V
$V_{IL(AC)}$	AC LOW-level input voltage (DDR3L)	CMD/ADD/CTRL inputs	–0.2	–	V_{REF} – 0.09	V
$V_{IH(DC)}$	DC HIGH-level input voltage (DDR3L)	CMD/ADD/CTRL inputs	V_{REF} + 0.09	–	V_{DD}	V
$V_{IL(DC)}$	DC LOW-level input voltage (DDR3L)	CMD/ADD/CTRL inputs	V_{SS}	–	V_{REF} – 0.09	V
$V_{IH(AC)\_DQ}$	AC HIGH-level input voltage (DDR3L)	DQ inputs	V_{REF} + 0.09	–	V_{DD} + 0.2	V
$V_{IL(AC)\_DQ}$	AC LOW-level input voltage (DDR3L)	DQ inputs	–0.2	–	V_{REF} – 0.09	V
$V_{IH(DC)\_DQ}$	DC HIGH-level input voltage (DDR3L)	DQ inputs	V_{REF} + 0.09	–	V_{DD}	V
$V_{IL(DC)\_DQ}$	DC LOW-level input voltage (DDR3L)	DQ inputs	V_{SS}	–	V_{REF} – 0.09	V
$V_{IH(CMOS)}$	HIGH-level input voltage	RESET#	0.65 x VDD	–	V_{DD}	V
$V_{IL(CMOS)}$	LOW-level input voltage	RESET#	0	–	0.35 x VDD	V
$V_{IL\ (Static)}$	Static LOW-level input voltage[3]	CK, CK#	–	–	0.35 x VDD	V
$V_{IX(AC)}$	Differential input crosspoint voltage range	CK, CK#	0.5xV_{DD} - 0.2	0.5 x V_{DD}	0.5xV_{DD} + 0.2	V
$V_{ID(AC)}$	Differential input voltage[4] (DDR3)	CK, CK#	0.2	–	V_{DD}	V
$V_{ID(AC)}$	Differential input voltage[d] (DDR3L)	CK, CK#	0.18	–	V_{DD}	V
$V_{IX(AC)\_DQS}$	Differential input crosspoint voltage range	DQS, DQS#	0.5xV_{DD} - 0.2	0.5 x V_{DD}	0.5xV_{DD} + 0.2	V
$V_{ID(AC)\_DQS}$	Differential input voltage[5] (DDR3)	DQS, DQS#	0.2	–	V_{DD}	V
$V_{ID(AC)\_DQS}$	Differential input voltage[e] (DDR3L)	DQS, DQS#	0.18	–	V_{DD}	V
I_{OH}	HIGH-level output current[6]	All CA outputs	-11	–	–	mA
I_{OL}	LOW-level output current	All CA outputs	11	–	–	mA
I_{OH}	HIGH-level output current	All DQ outputs	-10.7	–	–	mA
I_{OL}	LOW-level output current	All DQ outputs	10.7	–	–	mA
I_{OL_ERROUT}	LOW-level output current	Err_Out#	25	–	–	mA
I_{OL_EVENT}	LOW-level output current	EVENT	25	–	–	mA
V_{OD}	Differential re-driven clock swing	Yn, Yn#	0.45	–	V_{DD}	V

Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{OX}	Differential output crosspoint voltage	DQS, DQS#	$0.5xV_{DD} – 0.09$	–	$0.5xV_{DD} + 0.09$	V
$T_{case\ (max)}$	iMB Case temperature[7]		-	-	125[note8]	°C
V_{OL_ERROUT}	Output LOW voltage (Err_Out# pin)	IOL = 25 mA	-	-	0.4	V
V_{OL_EVENT}	Output LOW voltage (EVENT pin)	IOL = 25 mA	-	-	0.4	V
I_{I_RST}	Input current for RESET# pin	RESET#, VI = VDD or GND	-	-	±5	µA
I_{ID}	Input current for CMD, ADD, CNTRL and PAR_IN input pins	Data inputs1, VI = VDD or GND	-	-	±5	µA
I_{I_CK}	Input current for CK and CK# input pins	CK, CK#2; VI = VDD or GND	-5		150	µA

Notes:

1. VTT supply voltage specification is for DRAM portion of the LRDIMM (QCMD/QADDR/QCTRL/Yn/Yn# only;
2. DCKE[2:0], DCKE[3]/DODT[1], DODT[0], DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[7:0]#;
3. This specification applies only when both CK and CK# are actively driven LOW. It does not apply when CK/CK# are floating.
4. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
5. VID_DQS is the magnitude of the difference between the input level on DQS and the input level on DQS#.
6. Default settings
7. Measurement procedure JESD51-2
8. Since iMB silicon is bare die on FBGA package, the assumption is Tcase (max) is very close to silicon Tj (max). Hence, Tcase (max) of 125 °C is used for all speed grades.
9. Spec value is for each pin

DC CHARACTERISTICS DEFINITIONS (Recommended operating conditions unless otherwise noted, Tcase = 0 to 95 °C)

Symbol	Conditions	Units	Notes
IDD0	**Operating one bank active-precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2
IDD2P-S	**Precharge power-down current (slow exit);** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2P-F	**Precharge power-down current (fast exit);** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2Q	**Precharge quiet standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2N	**Precharge standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD3P	**Active power-down current;** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD3N	**Active standby current;** All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING;Data bus inputs are SWITCHING	mA	1, 2
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRAS-max(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2
IDD5B	**Burst refresh current;** tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD6	**Self refresh current;** CK and CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	mA	1, 3
IDD6ET	**Extended Temperature Range Self-Refresh Current;** CK and CK at 0V; CKE ≤ 0.2V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6=0 and A7=1	mA	1, 3
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	mA	1, 2

Notes:
1) Calculated values are from component data.
2) One module rank in the active IDD; the other ranks in IDD2P-S (slow exit)
3) All ranks in this IDD condition.

IDD CURRENT

DC CHARACTERISTICS CURRENTS 8-RANK 4Gbit 1.5V VDD

Symbol	DDR3-800	DDR3-1066	Unit
IDD0 (Note 1)	TBD	1280	mA
IDD1 (Note 1)	TBD	1360	mA
IDD2P-S (Note 2)	TBD	1080	mA
IDD2P-F (Note 2)	TBD	1080	mA
IDD2Q (Note 2)	TBD	1440	mA
IDD2N (Note 2)	TBD	1440	mA
IDD3P (Note 2)	TBD	1440	mA
IDD3N (Note 2)	TBD	2160	mA
IDD4R (Note 1)	TBD	1520	mA
IDD4W (Note 1)	TBD	1560	mA
IDD5B (Note 1)	TBD	1920	mA
IDD6 (Note 2)	TBD	1080	mA
IDD6ET (Note 2)	TBD	2016	mA
IDD7 (Note 1)	TBD	2000	mA

Notes:
1. One module rank in the active IDD, the other ranks in IDD2P-S (slow exit).
2. All ranks in this IDD condition.

DC CHARACTERISTICS CURRENTS 8-RANK 4Gbit 1.35V VDD

Symbol	DDR3-800	DDR3-1066	Unit
IDD0 (Note 1)	TBD	1280	mA
IDD1 (Note 1)	TBD	1360	mA
IDD2P-S (Note 2)	TBD	1080	mA
IDD2P-F (Note 2)	TBD	1080	mA
IDD2Q (Note 2)	TBD	1440	mA
IDD2N (Note 2)	TBD	1440	mA
IDD3P (Note 2)	TBD	1080	mA
IDD3N (Note 2)	TBD	1800	mA
IDD4R (Note 1)	TBD	1520	mA
IDD4W (Note 1)	TBD	1560	mA
IDD5B (Note 1)	TBD	1880	mA
IDD6 (Note 2)	TBD	1080	mA
IDD6ET (Note 2)	TBD	1080	mA
IDD7 (Note 1)	TBD	2000	mA

Notes:
1. One module rank in the active IDD, the other ranks in IDD2P-S (slow exit).
2. All ranks in this IDD condition.

CAPACITANCE

Symbol	Parameter	Conditions	Min		Max	Unit
C_I	Input capacitance, CA and CTRL inputs (with any IBT[3])	See Notes 1 and 2	0.7	-	1.2	pF
C_{CK}	Input capacitance, CK, CK#	See Note 1	0.7	-	1.2	pF
C_{IO}	Input/output capacitance	DQ, DQS and DQS#	1.4	-	2.1	pF
C_{IR}	Input capacitance, RESET#	$V_I = V_{DD}$ or GND; V_{DD} = 1.5V	-	-	3	pF

Notes:

1. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD and VSS applied and all other pins floating (except the pin under test, DCKE[2:0], DCKE[3]/DODT[1], RESET# and ODT[0] as necessary). VDD=1.5V/1.35V, VBIAS=VDD/2 and on-die termination off. The specified values are on die cap only (not including package cap).
2. Data inputs are DCKE[2:0], DCKE[3]/DODT[1], DODT[0], DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[7:0]#
3. Input Bus Termination on the command/address and control input-only pins on the iMB

DC and AC Specifications for the SMBus Interface

The specifications for the SMBus follow industry standards.

Host Interface Termination Specifications

CMD/ADDR/CTRL Input Bus Termination Requirement

Symbol	Parameter	DDR3/DDR3L-800/1066			Unit
		Min	Typ	Max	
$IBT_{(300)}$	Termination resistance	270	300	330	Ω
$IBT_{(200)}$	Termination resistance	180	200	220	Ω
$IBT_{(150)}$	Termination resistance	135	150	165	Ω
$IBT_{(100)}$	Termination resistance	90	100	110	Ω
IBT_{TOL}	Termination tolerance[1]	-10	-	10	%
ΔV_M	Deviation of V_M w.r.t. $V_{DD}/2$[3]	-	-	2.5	%

Notes:

1) Tolerance is defined as the deviation from the nominal value of the small signal input resistance. Measured from$0.2*V_{DD}$ to $0.8*V_{DD}$

2) Measure voltage ($V_{OUT} = V_M$) at test pin with no load ($I_{OUT} = 0$). $\Delta V_M = |2 *V_M/V_{DD} - 1| * 100\%$.

Host Interface Input Timing and DQ/DQS Output Timing

This section specifies various input timing for command/Address/Control/Clock, DQ/DQS, C/A setup and hold, Data setup and hold, initialization, control word write, power-down, write leveling, and RTT. In addition, it also covers DQ/DQS timing.

Host Interface Input Timing Parameters

Symbol	Parameter	DDR3-800		DDR3-1066						Unit
		Min	Max	Min	Max					
Input Clock Timing										
f_{clock}	Input clock frequency	300	810	300	810					MHz
f_{TEST}	Input clock frequency	70	300	70	300					MHz
t_{CH}/t_{CL}	Pulse duration, CK, CK# HIGH or LOW	0.4	0.6	0.4	0.6					t_{CK}[1]
Initialization Timing										
t_{INIT}	Duration of reset after stable VDD	200	-	200	-					µs
t_{ACT}	Time for VREF, DCKEx, DCSx to be stable before RESET# goes HIGH	8	-	8	-					t_{CK}

Symbol	Parameter	DDR3-800		DDR3-1066						Unit
		Min	Max	Min	Max					
t_{STAB}	PLL lock time (for Application Frequency Only)	6	-	6	-					µs
t_{QVREF}	QVREFCA/QVREFDQ voltage stable till RESET# goes HIGH	1	-	1	-					µs
Control Word & DRAM MRS Write Timing										
t_{MRD}	Control word to control word (or next command) programming delay	16	-	16	-					t_{CK}
t_{DRAM_MRS}	DRAM MRS to MRS Command programming delay	6		6						t_{CK}
Power Down Timing										
t_{InDIS}	Input buffers (except for CK/CK#, DCKEn, DODTn and RESET#) disable time after DCKE[1:0] is LOW	1	4	1	4					t_{CK}
t_{QDIS}	Output buffers (except for Yn/Yn#, QxCKEn, QxODTn) hi-z after QxCKEn is driven LOW	1.5	1.5	1.5	1.5					t_{CK}
t_{CKoff}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/CK# are driven LOW	5	-	5	-					t_{CK}
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after CK/CK# = LOW	2	-	2	-					t_{CK}
$t_{Fixedoutput}$	Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state)	1	3	1	3					t_{CK}
CMD/ADDR/CTL Inputs Timing										

Symbol	Parameter	DDR3-800		DDR3-1066						Unit
		Min	Max	Min	Max					
tIS (AC100)	Setup time[2] (DDR3)	100	-	100	-					ps
tIH (DC100)	Hold time[3] (DDR3)	100	-	100	-					ps
ODTH4	DODTn high time without write command or with write command and BC4	4	-	4	-					t_{CK}
ODTH8	DODTn high time without write command or with write command and BL8	8	-	8	-					t_{CK}
DQ Inputs Timing										
tDS (AC100)	Setup time[4] (DDR3)	45	-	45	-					ps
tDH (DC100)	Hold time[5] (DDR3)	45	-	45	-					ps
tDS (AC90)	Setup time (DDR3L)	55	-	55	-					ps
tDH (DC90)	Hold time (DDR3L)	55	-	55	-					ps
Data Strobe (DQS) Inputs Timing										
tWPRE	DQS, DQS# differential WRITE Preamble	0.9	-	0.9	-					t_{CK}
tWPST	DQS, DQS# differential WRITE Postamble	0.3	-	0.3	-					t_{CK}
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	0.45	0.55					t_{CK}
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	0.45	0.55					t_{CK}
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	-0.25	0.25					t_{CK}
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.2	-	0.2	-					t_{CK}
tDSH	DQS, DQS# falling edge hold time to CK, CK# rising edge	0.2	-	0.2	-					t_{CK}

Symbol	Parameter	DDR3-800		DDR3-1066						Unit
		Min	Max	Min	Max					
Write Leveling Inputs Timing										
tWLMRD	First DQS, DQS# rising edge after write leveling mode is programmed	40	-	40	-					nCK
tWLDQSEN	DQS, DQS# delay after write leveling mode is programmed	25	-	25	-					nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	325	-	245	-					Ps
tWLH	Write leveling hold time from rising CK, CK# crossing to rising DQS, DQS# crossing	325	-	245	-					Ps
RTT Inputs Timing										
tAON	RTT turn-on	-400	400	-300	300					Ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7					t_{CK}
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7					t_{CK}

Notes:

1. Clock cycle time
2. Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and first crossing of $V_{IH(ac)}$min. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value
3. Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value.
4. Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and first crossing of $V_{IH(ac)}$min. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max . If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value.
5. Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the

first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value.

Host Interface DQ/DQS Output Timing Parameters

Symbol	Parameter	DDR3 -800		DDR3-1066						Unit
		Min	Max	Min	Max					
DQ Output Timing										
tDQSQ	DQS, DQS# to DQ skew, per byte group, per access[1]	-	150	-	125					Ps
tQH	DQ output hold time from DQS, DQS#	0.45	-	0.45	-					t_{CK}[2]
Write Leveling Output Timing										
tWLO	Write leveling output delay	0	7.5	0	7.5					Ns
tWLOE	Write leveling output error	0	2	0	2					Ns
Data Strobe (DQS) Output Timing										
tRPRE	DQS, DQS# differential READ Preamble	0.9	-	0.9	-					t_{CK}
tRPST	DQS, DQS# differential READ Postamble	0.3	-	0.3	-					t_{CK}
tQSH	DQS, DQS# differential output high time	0.46	-	0.46	-					t_{CK}
tQSL	DQS, DQS# differential output low time	0.46	-	0.46	-					t_{CK}

Notes:
1. This skew represents the absolute output skew and contains the pad skew and package skew.
2. Clock cycle time

DRAM TIMING CHARACTERISTICS

Certain timing constraints need to be observed for sending commands to the DRAM's. The checking and optimizing of all the various timing requirements is simplified by the buffer observing the timing between two consecutive commands and refresh timing.