DDR3L
SODIMM
VR7PUxx6498xxx
Industrial Temperature

MODULE CONFIGURATIONS

Viking Part Number	Capacity	Module Configuration	Device Configuration	Device Package	Module Ranks	Performance	CAS Latency
VR7PU286498FBZyzT	1GB	128MX64	128Mx8	FBGA	1	PC3-6400	CL6 (6-6-6)
VR7PU286498FBAyzT	1GB	128MX64	128Mx8	FBGA	1	PC3-8500	CL7 (7-7-7)
VR7PU286498FBDyzT	1GB	128MX64	128Mx8	FBGA	1	PC3-10600	CL9 (9-9-9)
VR7PU286498FBFyzT	1GB	128MX64	128Mx8	FBGA	1	PC3-12800	CL11 (11-11-11)
VR7PU566498FBZyzT	2GB	256MX64	128Mx8	FBGA	2	PC3-6400	CL6 (6-6-6)
VR7PU566498FBAyzT	2GB	256MX64	128Mx8	FBGA	2	PC3-8500	CL7 (7-7-7)
VR7PU566498FBDyzT	2GB	256MX64	128Mx8	FBGA	2	PC3-10600	CL9 (9-9-9)
VR7PU566498FBFyzT	2GB	256MX64	128Mx8	FBGA	2	PC3-12800	CL11 (11-11-11)
VR7PU566498GBZyzT	2GB	256MX64	256Mx8	FBGA	1	PC3-6400	CL6 (6-6-6)
VR7PU566498GBAyzT	2GB	256MX64	256Mx8	FBGA	1	PC3-8500	CL7 (7-7-7)
VR7PU566498GBDyzT	2GB	256MX64	256Mx8	FBGA	1	PC3-10600	CL9 (9-9-9)
VR7PU566498GBFyzT	2GB	256MX64	256Mx8	FBGA	1	PC3-12800	CL11 (11-11-11)
VR7PU126498GBZyzT	4GB	512MX64	256Mx8	FBGA	2	PC3-6400	CL6 (6-6-6)
VR7PU126498GBAyzT	4GB	512MX64	256Mx8	FBGA	2	PC3-8500	CL7 (7-7-7)
VR7PU126498GBDyzT	4GB	512MX64	256Mx8	FBGA	2	PC3-10600	CL9 (9-9-9)
VR7PU126498GBFyzT	4GB	512MX64	256Mx8	FBGA	2	PC3-12800	CL11 (11-11-11)
VR7PU126498HBZyzT	4GB	512MX64	512Mx8	FBGA	1	PC3-6400	CL6 (6-6-6)
VR7PU126498HBAyzT	4GB	512MX64	512Mx8	FBGA	1	PC3-8500	CL7 (7-7-7)
VR7PU126498HBDyzT	4GB	512MX64	512Mx8	FBGA	1	PC3-10600	CL9 (9-9-9)
VR7PU126498HBFyzT	4GB	512MX64	512Mx8	FBGA	1	PC3-12800	CL11 (11-11-11)
VR7PU1G6498HBZyzT	8GB	1GX64	512Mx8	FBGA	2	PC3-6400	CL6 (6-6-6)
VR7PU1G6498HBAyzT	8GB	1GX64	512Mx8	FBGA	2	PC3-8500	CL7 (7-7-7)
VR7PU1G6498HBDyzT	8GB	1GX64	512Mx8	FBGA	2	PC3-10600	CL9 (9-9-9)
VR7PU1G6498HBFyzT	8GB	1GX64	512Mx8	FBGA	2	PC3-12800	CL11 (11-11-11)

Notes:
1. For part numbers containing an x, contact Viking for the complete PN.
2. y and z = Lowercase character(s) for DRAM vendor and die revisions and/or for customer specific locked BOM's.

Features

- JEDEC standard Power Supply
    - VDD = 1.35V (1.283V to 1.45V)
    - VDDSPD = +3.0V to +3.6V
- 204pin Small Outline Dual-In-Line Memory Module.
- 8 Internal Banks.
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11
- Programmable CAS Write Latency (CWL).
- Programmable Additive Latency (Posted CAS).
- Selectable BC4 or BL8 on-the-fly (OTF)
- Industrial Temperature: - 40 to +95°C (DRAM case)
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh. Self Refresh and Power Down Modes.
- Serial Presence Detect with EEPROM.
- On-DIMM Thermal Sensor.
- RoHS Compliant* (see last page)

Nomenclature

Module Standard	SDRAM Standard	Clock
PC3-6400	DDR3-800	400MHz
PC3 -8500	DDR3-1066	533MHz
PC3-10600	DDR3-1333	667MHz
PC3-12800	DDR3-1600	800MHz

PIN CONFIGURATIONS

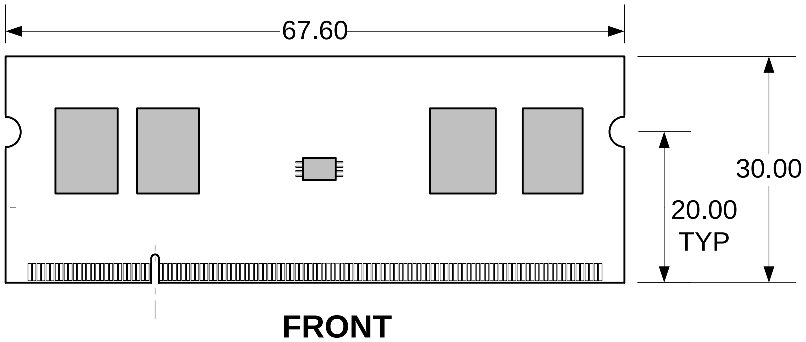
Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VREFDQ	2	Vss	53	DQ19	54	Vss	105	VDD	106	VDD	157	DQ42	158	DQ46
3	Vss	4	DQ4	55	Vss	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	RAS#	161	Vss	162	Vss
7	DQ1	8	Vss	59	DQ25	60	Vss	111	VDD	112	VDD	163	DQ48	164	DQ52
9	Vss	10	DQS0#	61	Vss	62	DQS3#	113	WE#	114	S0#	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	CAS#	116	ODT0	167	Vss	168	Vss
13	Vss	14	Vss	65	Vss	66	Vss	117	VDD	118	VDD	169	DQS6#	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13	120	ODT1	171	DQS6	172	Vss
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	S1#	122	NC	173	Vss	174	DQ54
19	Vss	20	Vss	71	Vss	72	Vss	123	VDD	124	VDD	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	VREFCA	177	DQ51	178	Vss
23	DQ9	24	DQ13	75	VDD	76	VDD	127	Vss	128	Vss	179	Vss	180	DQ60
25	Vss	26	Vss	77	NC	78	A15	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	DQS1#	28	DM1	79	BA2	80	A14	131	DQ33	132	DQ37	183	DQ57	184	Vss
29	DQS1	30	RESET#	81	VDD	82	VDD	133	Vss	134	Vss	185	Vss	186	DQS7#
31	Vss	32	Vss	83	A12/BC#	84	A11	135	DQS4#	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	Vss	189	Vss	190	Vss
35	DQ11	36	DQ15	87	VDD	88	VDD	139	Vss	140	DQ38	191	DQ58	192	DQ62
37	Vss	38	Vss	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	Vss	195	Vss	196	Vss
41	DQ17	42	DQ21	93	VDD	94	VDD	145	Vss	146	DQ44	197	SA0	198	EVENT#
43	Vss	44	Vss	95	A3	96	A2	147	DQ40	148	DQ45	199	VDDSPD	200	SDA
45	DQS2#	46	DM2	97	A1	98	A0	149	DQ41	150	Vss	201	SA1	202	SCL
47	DQS2	48	Vss	99	VDD	100	VDD	151	Vss	152	DQS5#	203	Vtt	204	Vtt
49	Vss	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	CK0#	104	CK1#	155	Vss	156	Vss				

PIN FUNCTION DESCRIPTION

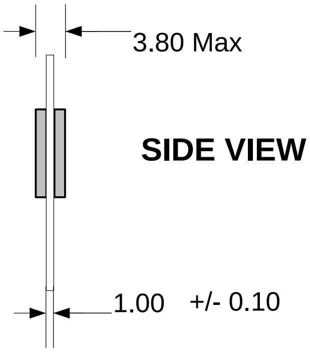
SYMBOL	TYPE	POLARITY	DESCRIPTION
CK0, CK1	IN	Positive Edge	Positive lines of the differential pairs of system clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CK0#, CK1#	IN	Negative Edge	Negative lines of the differential pairs of system clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[1:0]#	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS#, CAS#, WE#	IN	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operation to be executed by the SDRAM.
VREFDQ	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
VREFCA	Supply		Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S1#, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	-	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[15:13, 12/BC,11, 10/AP,9:0]	IN	-	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for ''BL on the fly'' during CAS# command. The address inputs also provide the op-code during Mode Register Set commands.
DQ [63:0],	I/O	-	Data and Check Bit Input/Output pins
VDD, VSS	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
DM [7:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
VDD, VSS	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
VTT	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[7:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS [7:0]#	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA [1:0]	IN	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pullup.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDDSPD on the system planar to act as a pullup.
EVENT#	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the EVENT pin on TS/SPD part.
VDDSPD	Supply	-	Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET#	IN		This signal resets the DDR3 SDRAM.

MECHANICAL OUTLINE SINGLE RANK

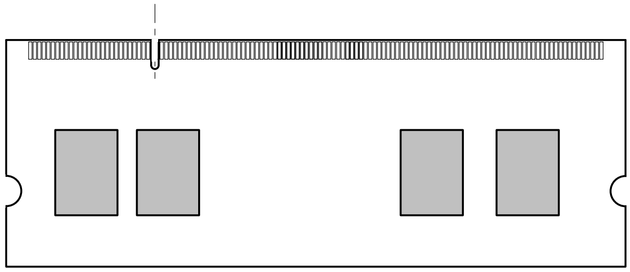
Dimensions are in mm. Tolerance is +/- 0.127, unless otherwise stated.



FRONT



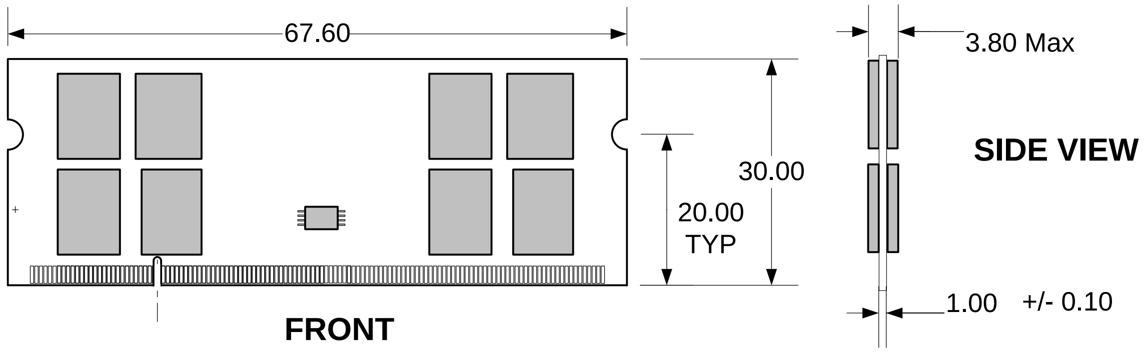
SIDE VIEW

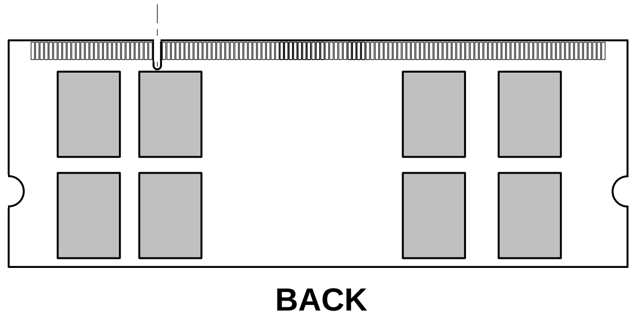


BACK

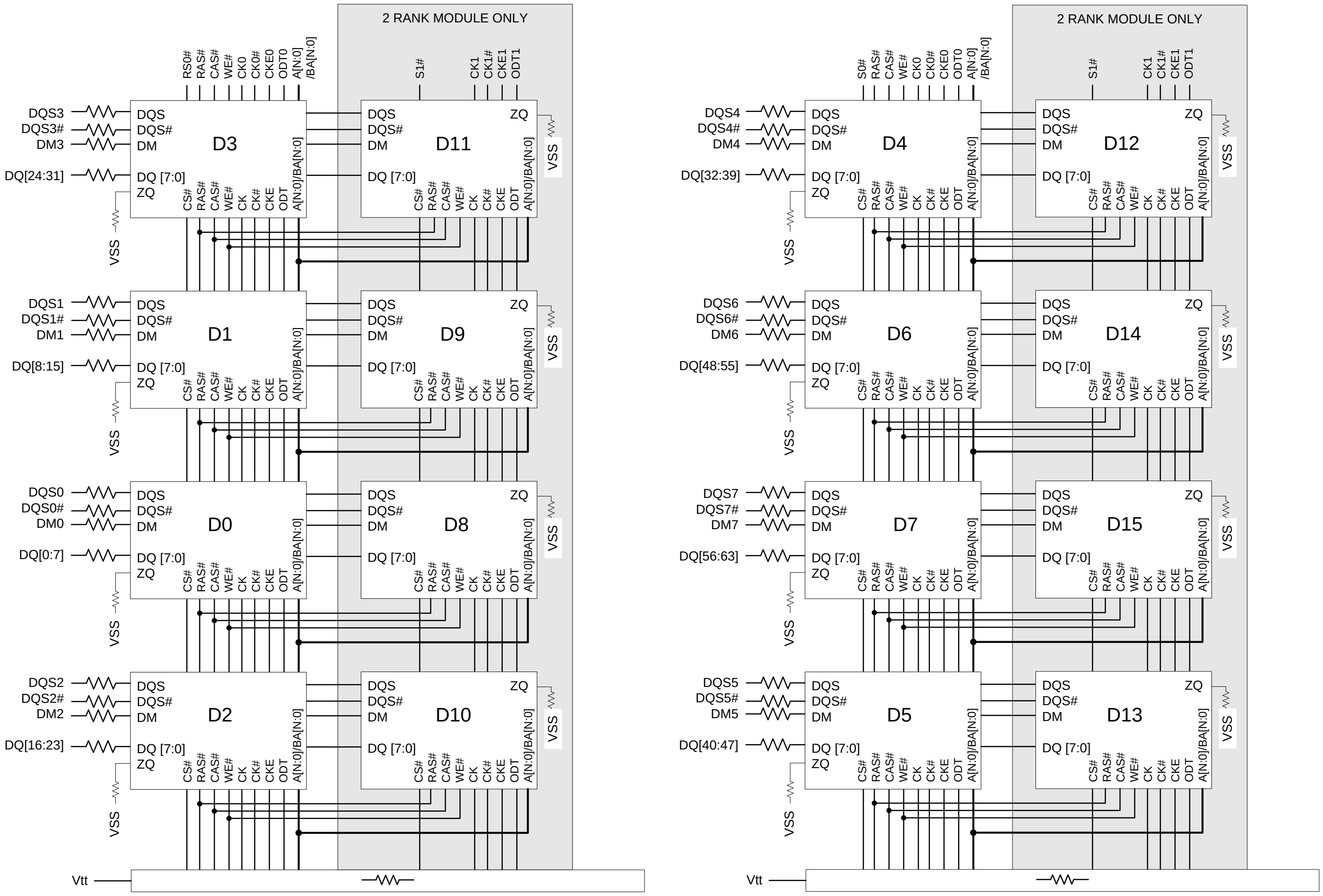
MECHANICAL OUTLINE DUAL RANK

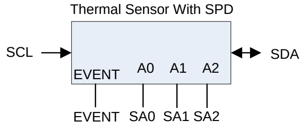
Dimensions are in mm. Tolerance is +/- 0.127, unless otherwise stated.

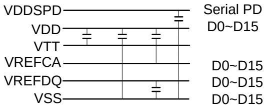




FUNCTIONAL BLOCK DIAGRAM







Notes:
The resistor values may vary depending on systems application

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to GND	Vin, Vout	-0.4 ~ 1.975	V
Voltage on VDD supply relative to GND	VDD	-0.4 ~ 1.975	V
Voltage on VDDQ supply relative to GND	VDDQ	-0.4 ~ 1.975	V
Storage temperature	TSTG	-55 ~ +100	°C

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (SSTL_1.35)

Recommended operating conditions (Voltages referenced to GND, Tcase = 0 to 95°C)

Parameter		Symbol	Min.	Max.	Unit	Notes
Case Temperature_Commercial		Tcase$_C$	0	95	ºC	5
Case Temperature_Industrial (I-Temp)		Tcase$_I$	-40	95	ºC	5
Supply voltage		VDD	1.283	1.45	V	1, 2
Supply voltage for DQ, DQS		VDDQ	1.283	1.45	V	1, 2
Reference Voltage for DQ, DM inputs		VREFDQ(DC)	0.49 x VDD	0.51 x VDD	V	3, 4
Reference Voltage for ADD, CMD inputs		VREFCA(DC)	0.49 x VDD	0.51 x VDD	V	3, 4
Terminal Voltage		VTT	0.49 x VDD	0.51 x VDD	V	3, 4
EEPROM Supply Voltage		VDDSPD	3.0	3.6	V	
Input high voltage		VIH(AC)	VREF + 0.175	-	V	
		VIH(DC)	VREF + 0.100	VDD		
Input low voltage		VIL(AC)	-	VREF - 0.175	V	
		VIL(DC)	VSS	VREF – 0.100		
Input leakage current	Single Rank	IIL	-16	16	µA	
	Dual Rank		-32	32		
Output leakage current	Single Rank	IOL	-5	5	µA	
	Dual Rank		-10	10		

Notes:

1. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together
2. Under all conditions VDDQ must be less than or equal to VDD.
3. The ac peak noise on VREF may not allow VREF to deviate from VREF.DC by more than ±1% VDD (for reference: approx. ± 15 mV).
4. For reference: approx. VDD/2 ± 15 mV.
5. Refresh rate required to be doubled (tREFI = 3.9µs) when 85°C < TC < 95°C.

DEVICE CAPACITANCE

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS,TDQS#)	CIO	1.5	3	1.5	2.7	1.5	2.5	1.5	2.3	pF	1,2,3
Input capacitance, CK and CK#	CCK	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
Input capacitance delta, CK and CK#	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input/output capacitance delta DQS and DQS#	CDDQS	0	0.2	0	0.2	0	0.15	0	0.15	pF	2,3,5
Input capacitance, (CTRL, ADD, CMD input-only pins)	CI	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	pF	2,3,6
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	pF	2,3,7

Notes:

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.35V, VBIAS=VDD/2 and on die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of CCK-CCK#
5. Absolute value of CIO(DQS)-CIO(DQS#)
6. CI applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. Maximum external load capacitance on ZQ pin: 5 pF.

DC CHARACTERISTICS DEFINITION (Recommended operating conditions unless otherwise noted, Tcase 0 to 85 °C

Symbol	Conditions	Units	Notes
IDD0	**Operating one bank active-precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 2
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2
IDD2P-S	**Precharge power-down current (slow exit);** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2P-F	**Precharge power-down current (fast exit);** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2Q	**Precharge quiet standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD2N	**Precharge standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD3P	**Active power-down current;** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	1, 3
IDD3N	**Active standby current;** All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING;Data bus inputs are SWITCHING	mA	1, 2
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRAS-max(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	1, 2
IDD5B	**Burst refresh current;** tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	1, 3
IDD6	**Self refresh current;** CK and CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	mA	1, 3
IDD6ET	**Extended Temperature Range Self-Refresh Current;** CK and CK at 0V; CKE ≤ 0.2V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6=0 and A7=1	mA	1, 3
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	mA	1, 2

Notes:

1) Calculated values are from component data.
2) One module rank in the active IDD; the other rank in IDD2P-S (slow exit)
3) All ranks in this IDD condition.

DC CHARACTERISTICS CURRENTS for SINGLE RANK with 1Gbit device

Symbol	DDR3-1066	DDR3-1333	Unit
IDD0	360	405	mA
IDD1	450	495	mA
IDD2P-S	90	90	mA
IDD2P-F	135	135	mA
IDD2Q	180	180	mA
IDD2N	180	225	mA
IDD3P	225	225	mA
IDD3N	360	405	mA
IDD4R	720	810	mA
IDD4W	720	855	mA
IDD5B	990	990	mA
IDD6	90	90	mA
IDD7	1215	1485	mA

DC CHARACTERISTICS CURRENTS for SINGLE RANK with 2Gbit devices

Symbol	DDR3-1066	DDR3-1333	DDR3-1600	Unit
IDD0	450	495	540	mA
IDD1	540	585	630	mA
IDD2P-S	108	108	108	mA
IDD2P-F	180	180	180	mA
IDD2Q	225	270	270	mA
IDD2N	225	270	270	mA
IDD3P	225	270	270	mA
IDD3N	405	450	495	mA
IDD4R	810	945	1080	mA
IDD4W	900	1215	1350	mA
IDD5B	1485	1485	1530	mA
IDD6	108	108	108	mA
IDD7	1440	1755	1800	mA

DC CHARACTERISTICS CURRENTS for SINGLE RANK with 4Gbit devices

Symbol	DDR3-1066	DDR3-1333	DDR3-1600	Unit
IDD0	360	360	405	mA
IDD1	450	450	495	mA
IDD2P-S	135	135	135	mA
IDD2P-F	135	135	135	mA
IDD2Q	180	180	180	mA
IDD2N	180	180	180	mA
IDD3P	135	180	180	mA
IDD3N	225	270	270	mA
IDD4R	630	765	900	mA
IDD4W	675	765	945	mA
IDD5B	1035	1305	1305	mA
IDD6	135	135	135	mA
IDD7	1170	1485	1530	mA

DC CHARACTERISTICS CURRENTS for DUAL RANK with 1Gbit devices

Symbol	DDR3-1066	DDR3-1333	Unit
IDD0	720	810	mA
IDD1	900	990	mA
IDD2P-S	180	180	mA
IDD2P-F	270	270	mA
IDD2Q	360	360	mA
IDD2N	360	450	mA
IDD3P	450	450	mA
IDD3N	720	810	mA
IDD4R	1440	1620	mA
IDD4W	1440	1710	mA
IDD5B	1980	1980	mA
IDD6	180	180	mA
IDD7	2430	2970	mA

DC CHARACTERISTICS CURRENTS for DUAL RANK with 2Gbit devices

Symbol	DDR3-1066	DDR3-1333	DDR3-1600	Unit
IDD0	900	990	1080	mA
IDD1	1080	1170	1260	mA
IDD2P-S	216	216	216	mA
IDD2P-F	360	360	360	mA
IDD2Q	450	540	540	mA
IDD2N	450	540	540	mA
IDD3P	450	540	540	mA
IDD3N	810	900	990	mA
IDD4R	1620	1890	2160	mA
IDD4W	1800	2430	2700	mA
IDD5B	2970	2970	3060	mA
IDD6	216	216	216	mA
IDD7	2880	3510	3600	mA

DC CHARACTERISTICS CURRENTS for DUAL RANK with 4Gbit devices

Symbol	DDR3-1066	DDR3-1333	DDR3-1600	Unit
IDD0	720	720	810	mA
IDD1	900	900	990	mA
IDD2P-S	270	270	270	mA
IDD2P-F	270	270	270	mA
IDD2Q	360	360	360	mA
IDD2N	360	360	360	mA
IDD3P	270	360	360	mA
IDD3N	450	540	540	mA
IDD4R	1260	1530	1800	mA
IDD4W	1350	1530	1890	mA
IDD5B	2070	2610	2610	mA
IDD6	270	270	270	mA
IDD7	2340	2970	3060	mA

AC CHARACTERISTICS

Refresh parameters by device density

Parameter	Symbol		1Gb	2Gb	4Gb	8Gb	Units	Notes
REF command to ACT or REF command time	tRFC		110	160	260	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ TCASE ≤ 85 °C	7.8	7.8	7.8	7.8	µs	
		85 °C < TCASE ≤ 95 °C	3.9	3.9	3.9	3.9	µs	1

Note: 1) Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

DDR3-800 Speed Bins and Operating Conditions

Speed Bin			DDR3-800		Unit	Notes
CL-nRCD-nRP			6-6-6			
Parameter		Symbol	min	max		
Internal read command to first data		*tAA*	15	20	ns	
ACT to internal read or write delay time		*tRCD*	15	—	ns	
PRE command period		*tRP*	15	—	ns	
ACT to ACT or REF command period		*tRC*	52.5	—	ns	
ACT to PRE command period		*tRAS*	37.5	9 * tREFI	ns	
CL = 6	CWL = 5	*tCK(AVG)*	2.5	3.3	ns	1, 2, 3
Supported CL Settings			6		*nCK*	13
Supported CWL Settings			5		*nCK*	

DDR3L-1066 Speed Bins and Operating Conditions

Speed Bin			DDR3L-1066		Unit	Note
CL-nRCD-nRP			7-7-7			
Parameter		Symbol	min	max		
Internal read command to first data		*tAA*	13.125	20	ns	
ACT to internal read or write delay time		*tRCD*	13.125	—	ns	
PRE command period		*tRP*	13.125	—	ns	
ACT to ACT or REF command period		*tRC*	50.625	—	ns	
ACT to PRE command period		*tRAS*	37.5	9 * tREFI	ns	
CL = 6	CWL = 5	*tCK(AVG)*	2.5	3.3	ns	1,2,3,6,
	CWL = 6	*tCK(AVG)*	Reserved		ns	1,2,3,4,
CL = 7	CWL = 5	*tCK(AVG)*	Reserved		ns	4,
	CWL = 6	*tCK(AVG)*	1.875	< 2.5	ns	1,2,3,4,
CL = 8	CWL = 5	*tCK(AVG)*	Reserved		ns	4,
	CWL = 6	*tCK(AVG)*	1.875	< 2.5	ns	1,2,3,
Supported CL Settings			6, 7, 8		*nCK*	13
Supported CWL Settings			5, 6		*nCK*	

DDR3L-1333 Speed Bins and Operating Conditions

Speed Bin			DDR3L-1333		Unit	Note
CL-nRCD-nRP			9-9-9			
Parameter		Symbol	min	max		
Internal read command to first data		*tAA*	13.5 (13.125)5,11	20	ns	
ACT to internal read or write delay time		*tRCD*	13.5 (13.125)5,11	—	ns	
PRE command period		*tRP*	13.5 (13.125)5,11	—	ns	
ACT to ACT or REF command period		*tRC*	49.5 (49.125)5,11	—	ns	
ACT to PRE command period		*tRAS*	36	9 * tREFI	ns	
CL = 6	CWL = 5	*tCK(AVG)*	2.5	3.3	ns	1,2,3,7
	CWL = 6	*tCK(AVG)*	Reserved		ns	1,2,3,4,7
	CWL = 7	*tCK(AVG)*	Reserved		ns	4
CL = 7	CWL = 5	*tCK(AVG)*	Reserved		ns	4
	CWL = 6	*tCK(AVG)*	1.875	< 2.5	ns	1,2,3,4,7
			(Optional)5,11			
	CWL = 7	*tCK(AVG)*	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	*tCK(AVG)*	Reserved		ns	4
	CWL = 6	*tCK(AVG)*	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	*tCK(AVG)*	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	*tCK(AVG)*	Reserved		ns	4
	CWL = 7	*tCK(AVG)*	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	*tCK(AVG)*	Reserved		ns	4
	CWL = 7	*tCK(AVG)*	1.5	<1.875	ns	1,2,3
			(Optional)			
Supported CL Settings			6, 8, (7), 9, (10)		*nCK*	
Supported CWL Settings			5, 6, 7		*nCK*	

DDR3L-1600 Speed Bins and Operating Conditions

Speed Bin			DDR3L-1600		Unit	Note
CL-nRCD-nRP			11-11-11			
Parameter		Symbol	min	max		
Internal read command to first data		*tAA*	13.75 (13.125)9	20	ns	
ACT to internal read or write delay time		*tRCD*	13.75 (13.125)9	—	ns	
PRE command period		*tRP*	13.75 (13.125)9	—	ns	
ACT to ACT or REF command period		*tRC*	48.75 (48.125)9	—	ns	
ACT to PRE command period		*tRAS*	35	9 * tREFI	ns	
CL = 6	CWL = 5	*tCK(AVG)*	2.5	3.3	ns	1,2,3,7
	CWL = 6	*tCK(AVG)*	Reserved		ns	1,2,3,4,7
	CWL = 7	*tCK(AVG)*	Reserved		ns	4
CL = 7	CWL = 5	*tCK(AVG)*	Reserved		ns	4
	CWL = 6	*tCK(AVG)*	1.875	< 2.5	ns	1,2,3,4,7
			(Optional)5,11			
	CWL = 7	*tCK(AVG)*	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	*tCK(AVG)*	Reserved		ns	4
	CWL = 6	*tCK(AVG)*	1.875	< 2.5	ns	1,2,3,7

Speed Bin			DDR3L-1600		Unit	Note
CL-nRCD-nRP			11-11-11			
Parameter		Symbol	min	max		
	CWL = 7	*tCK(AVG)*	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	*tCK(AVG)*	Reserved		ns	4
	CWL = 7	*tCK(AVG)*	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	*tCK(AVG)*	Reserved		ns	4
	CWL = 7	*tCK(AVG)*	1.5	<1.875	ns	1,2,3
CL = 11	CWL = 5, 6, 7	*tCK(AVG)*	Reserved		ns	4
	CWL = 8	*tCK(AVG)*	1.25	<1.5	ns	1,2,3,9
Supported CL Settings			6, 8, 7, 9, 10, 11		*nCK*	
Supported CWL Settings			5, 6, 7, 8		*nCK*	

DDR3-1866 Speed Bins and Operating Conditions

Speed Bin			DDR3-1866		Unit	Note
CL-nRCD-nRP			13-13-13			
Parameter		Symbol	min	max		
Internal read command to first data		*tAA*	13.91 (13.125)10	20	ns	
ACT to internal read or write delay time		*tRCD*	13.91 (13.125)10	—	ns	
PRE command period		*tRP*	13.91 (13.125)10	—	ns	
ACT to ACT or REF command period		*tRC*	47.91 (48.125)10	—	ns	
ACT to PRE command period		*tRAS*	34	9 * tREFI	ns	
CL = 6	CWL = 5	*tCK(AVG)*	2.5	3.3	ns	1,2,3,8
	CWL = 6	*tCK(AVG)*	Reserved		ns	1,2,3,4,8
	CWL = 7,8,9	*tCK(AVG)*	Reserved		ns	4
CL = 7	CWL = 5	*tCK(AVG)*	Reserved		ns	4
	CWL = 6	*tCK(AVG)*	1.875	2.5	ns	1,2,3,4,8
			(Optional)5,11			
	CWL = 7,8,9	*tCK(AVG)*	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	*tCK(AVG)*	Reserved		ns	4
	CWL = 6	*tCK(AVG)*	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	*tCK(AVG)*	Reserved		ns	1,2,3,4,8
	CWL = 8,9	*tCK(AVG)*	Reserved		ns	4
CL = 9	CWL = 5,6	*tCK(AVG)*	Reserved		ns	4
	CWL = 7	*tCK(AVG)*	1.5	1.875	ns	1,2,3,4,8
	CWL = 8	*tCK(AVG)*	Reserved		ns	4
	CWL = 9	*tCK(AVG)*	Reserved		ns	4
CL = 10	CWL = 5,6,	*tCK(AVG)*	Reserved		ns	4
	CWL = 7	*tCK(AVG)*	1.5	<1.875	ns	1,2,3,8
	CWL = 8	*tCK(AVG)*	Reserved		ns	1,2,3,4,8
CL = 11	CWL = 5,6,7	*tCK(AVG)*	Reserved		ns	4
	CWL = 8	*tCK(AVG)*	1.25	1.5	ns	1,2,3,8
	CWL = 9	*tCK(AVG)*	Reserved		ns	1,2,3,4
CL = 12	CWL = 5, 6, 7,8	*tCK(AVG)*	Reserved		ns	4
	CWL = 9	*tCK(AVG)*	1.25	<1.5	ns	*1,2,3,4*

Speed Bin			DDR3-1866		Unit	Note
CL-nRCD-nRP			**13-13-13**			
Parameter		**Symbol**	**min**	**max**		
CL = 13	CWL = 5,6,7,8	*tCK(AVG)*	Reserved		ns	4
	CWL = 9	*tCK(AVG)*	1.071	<1.25	ns	1,2,3,9
Supported CL Settings			6, 8, 7, 9, 10, 11,13		*nCK*	
Supported CWL Settings			5, 6, 7, 8, 9		*nCK*	

Notes:

1. Absolute Specification (TOPER; VDDQ = VDD = 1.35V (1.283V to 1.45V));
2. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
3. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07, or 0.935 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
4. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.935 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
5. 'Reserved' settings are not allowed. User must program a different value.
6. 'Optional' settings allow certain devices in the industry to support this setting; however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
7. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. For devices supporting optional down binning to CL=7 and CL=9, tAA/tRCD/tRPmin must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21, 23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.

Timing Parameters

Speed		DDR3L-800		DDR3L-1066		DDR3L-1333		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OF F)	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table					ps		
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-100	100	-90	90	-80	80	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-90	90	-80	80	-70	70	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160	ps		
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	180		160		140	ps		
Cumulative error across 2 cycles	tERR(2per)	- 147	147	- 132	132	- 118	118	ps	
Cumulative error across 3 cycles	tERR(3per)	- 175	175	- 157	157	- 140	140	ps	
Cumulative error across 4 cycles	tERR(4per)	- 194	194	- 175	175	- 155	155	ps	
Cumulative error across 5 cycles	tERR(5per)	- 209	209	- 188	188	- 168	168	ps	
Cumulative error across 6 cycles	tERR(6per)	- 222	222	- 200	200	- 177	177	ps	
Cumulative error across 7 cycles	tERR(7per)	- 232	232	- 209	209	- 186	186	ps	
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max					ps		24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26
Data Timing									
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	ps	13
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, CK	tLZ(DQ)	-800	400	-600	300	-500	250	ps	13,14, f
DQ high-impedance time from CK, CK	tHZ(DQ)	-	400	-	300	-	250	ps	13,14, f
Data setup time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDS(base)	75	-	25	-	30	-	ps	d, 17
Data hold time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDH(base)	150	-	100	-	65	-	ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	ps	28
Data Strobe Timing									
DQS, DQS READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	tCK	13, 19, g
DQS, DQS differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	tCK	11, 13, b
DQS, DQS output high time	tQSH	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g
DQS, DQS output low time	tQSL	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g
DQS, DQS WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	
DQS, DQS WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK	
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-400	400	-300	300	-255	255	ps	13,f
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-800	400	-600	300	-500	250	ps	13,14,f
DQS, DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	400	-	300	-	250	ps	12,13,14
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	29, 31
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30, 31
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)	c
DQS,DQS falling edge setup time to CK, CK rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32
DQS,DQS falling edge hold time to CK, CK rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32

Timing Parameters (Cont.)

Speed		DDR3L-800		DDR3L-1066		DDR3L-1333		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-	max (12nCK,15ns)	-		
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See 13.3 " Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin" on page 37						ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-	max (4nCK,6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	ns	e
Command and Address setup time to CK, CK referenced to VIH(AC) / VIL(AC) levels	tIS(base)	200	-	125	-	65	-	ps	b,16
Command and Address hold time from CK, CK referenced to VIH(AC) / VIL(AC) levels	tIH(base)	275	-	200	-	140	-	ps	b,16
Command and Address setup time to CK, CK referenced to VIH(AC) / VIL(AC) levels	tIS(base) AC150	200 + 150	-	125 + 150	-	65+125	-	ps	b,16,27
Control & Address Input pulse width for each input	tIPW	900	-	780	-	620	-	ps	28
Calibration Timing									
Power-up and RESET calibration time	tZQinitI	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK	
Normal operation short calibration time	tZQCS	64	-	64	-	64	-	nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		

Timing Parameters(Cont.)

Speed		DDR3L-800		DDR3L-1066		DDR3L-1333		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Exit Power Down with DLL on to any valid com-mand;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to com-mands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK, 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK	10
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-		20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timing									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns	
ODT turn-on	tAON	-400	400	-300	300	-250	250	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing									
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK	3
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK	3
Setup time for tDQSS latch	tWLS	325	-	245	-	195	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	325	-	245	-	195	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

Timing Parameters (Cont.)

Speed		DDR3L-1600		DDR3L-1866				Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OF F)	8	-	8	-			ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table					ps		
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max			ps	

Speed		DDR3L-1600		DDR3L-1866				Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53			tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53			tCK(avg)	
Clock Period Jitter	tJIT(per)	-70	70	-60	60			ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-50	50			ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140		120			ps		
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		100			ps		
Cumulative error across 2 cycles	tERR(2per)	- 103	103	- 88	88			ps	
Cumulative error across 3 cycles	tERR(3per)	- 122	122	- 105	105			ps	
Cumulative error across 4 cycles	tERR(4per)	- 136	136	- 117	117			ps	
Cumulative error across 5 cycles	tERR(5per)	- 147	147	- 126	126			ps	
Cumulative error across 6 cycles	tERR(6per)	- 155	155	- 133	133			ps	
Cumulative error across 7 cycles	tERR(7per)	- 163	163	- 139	139			ps	
Cumulative error across 8 cycles	tERR(8per)	- 169	169	- 145	145			ps	
Cumulative error across 9 cycles	tERR(9per)	- 175	175	- 150	150			ps	
Cumulative error across 10 cycles	tERR(10per)	- 180	180	- 154	154			ps	
Cumulative error across 11 cycles	tERR(11per)	- 184	184	- 158	158			ps	
Cumulative error across 12 cycles	tERR(12per)	- 188	188	- 161	161			ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max					ps		24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-			tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-			tCK(avg)	26
Data Timing									
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	100	-	85			ps	13
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-			tCK(avg)	13, g
DQ low-impedance time from CK, CK	tLZ(DQ)	-450	225	-390	195			ps	13,14, f
DQ high-impedance time from CK, CK	tHZ(DQ)	-	225	-	195			ps	13,14, f
Data setup time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDS(base)	10	-	-	-			ps	d, 17
Data hold time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDH(base)	-	-	0	-			ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	360	-	320	-			ps	28
Data Strobe Timing									
DQS, DQS READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19			tCK	13, 19, g
DQS, DQS differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11			tCK	11, 13, b
DQS, DQS output high time	tQSH	0.4	-	0.4	-			tCK(avg)	13, g
DQS, DQS output low time	tQSL	0.4	-	0.4	-			tCK(avg)	13, g
DQS, DQS WRITE Preamble	tWPRE	0.9	-	0.9	-			tCK	
DQS, DQS WRITE Postamble	tWPST	0.3	-	0.3	-			tCK	
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-225	225	-195	195			ps	13,f
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195			ps	13,14,f
DQS, DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195			ps	12,13,14
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55			tCK	29, 31
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55			tCK	30, 31
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.27	0.27	-0.27	0.27			tCK(avg)	c
DQS,DQS falling edge setup time to CK, CK rising edge	tDSS	0.9	Note 19	0.18	-			tCK(avg)	c, 32
DQS,DQS falling edge hold time to CK, CK rising edge	tDSH	0.3	Note 11	0.18	-			tCK(avg)	c, 32

Timing Parameters (Cont.)

Speed		DDR3L-1600		DDR3L-1866				Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-			nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-				e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-				e,18
WRITE recovery time	tWR	15	-	15	-			ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-			nCK	
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-				
CAS# to CAS# command delay	tCCD	4	-	4	-			nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-			nCK	22
ACTIVE to PRECHARGE command period	tRAS	See " Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin"						ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,6ns)	-	max (4nCK,5ns)	-				e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,7.5ns)	-	max (4nCK,6ns)	-				e
Four activate window for 1KB page size	tFAW	30	-	27	-			ns	e
Four activate window for 2KB page size	tFAW	40	-	35	-			ns	e
Command and Address setup time to CK, CK referenced to VIH(AC) / VIL(AC) levels	tIS(base)	170	-	-	-			ps	b,16
Command and Address hold time from CK, CK referenced to VIH(AC) / VIL(AC) levels	tIH(base)	120	-	100	-			ps	b,16
Command and Address setup time to CK, CK referenced to VIH(AC) / VIL(AC) levels	tIS(base) AC150	-	-	-	-			ps	b,16,27
Control & Address Input pulse width for each input	tIPW	560	-	535	-			ps	28
Calibration Timing									
Power-up and RESET calibration time	tZQinitI	512	-	Max(512nCK,640ns)	-			nCK	
Normal operation Full calibration time	tZQoper	256	-	Max(256nCK,320ns)	-			nCK	
Normal operation short calibration time	tZQCS	64	-	Max(64nCK,80ns)	-			nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		

Timing Parameters(Cont.)

Speed		DDR3L-1600		DDR3L-1866				Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Power Down Timing									
Exit Power Down with DLL on to any valid com-mand;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 6ns)	-	max (3nCK, 6ns)	-				
Exit Precharge Power Down with DLL frozen to com-mands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-				2
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-				
Command pass disable delay	tCPDED	1	-	1	-			nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI			tCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-			nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-			nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	RL + 4 +1	-				
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-			nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR +1	-	WL + 4 +WR +1	-			nCK	10
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-			nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-			nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-				20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-				
ODT Timing									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-			nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-			nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5			ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5			ns	
ODT turn-on	tAON	-225	225	-195	195			ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7			tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7			tCK(avg)	f
Write Leveling Timing									
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-			tCK	3
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-			tCK	3
Setup time for tDQSS latch	tWLS	165	-	140	-			ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	165	-	140	-			ps	
Write leveling output delay	tWLO	0	7.5	0	7.5			ns	
Write leveling output error	tWLOE	0	2	0	2			ns	

18.1 Jitter Notes

1. Unit ’tCK(avg)’ represents the actual tCK(avg) of the input clock under operation. Unit ’nCK’ represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.
2. These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
3. These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)) crossing to its respective clock signal (CK, CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
4. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing. Specific Note e For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.
5. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!) Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.
6. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)= 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

18.2 Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON see "Device Operation"
8. For definition of RTT turn-off time tAOF see "Device Operation".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. Device Operation.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is valid for RON34
14. Single ended signal parameter.
15. tREFI depends on TOPER
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). FOr input only pins except RESET, VREF(DC)=VREFCA(DC). See "Address/ Command Setup, Hold and Derating"
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS differential slew rate. Note for DQ and DM signals, VREF(DC)= VREFDQ(DC). For input only pins except RESET, VREF(DC)=VREFCA(DC). See "Data Setup, Hold and Slew Rate Derating"
18. Start of internal write transaction is defined as follows ;
    For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
    For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
    For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side. See "Device Operation"
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation".
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ’Output Driver Voltage and Temperature Sensitivity’ and ’ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens x Tdriftrate}) + (\text{VSens x Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% /°C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \text{ x } 1) + (0.15 \text{ x } 15)} = 0.133 \sim\sim 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC)
29. tDQSL describes the instantaneous differential input low pulse width on DQS-DQS, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS-DQS, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
32. tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
Preliminary	July 13, 2012	Preliminary Release.	
A	January 18, 2013	Added 8GB PN's. Removed PN's with CL 8 and CL10. Update company name	
A1	April 25, 2013	Added tolerance to PCB thickness on mechanical drawing	
A2	June 29, 2013	Corrections: Pin 45 is DQS2 should be DQS2# Pin 78 is A153 should be A15 Pin 80 is A143 should be A14 Pin 119 is A133 should be A13 Revised mechanical drawing to show dimension in mm and a nominal thickness with tolerance	
A3	August 1, 2013	Add 4GB 1 rank PN's	
A4	12-Dec-13	Revised the tRFC for 4Gb from 300ns to 260ns	Chanhee Park
A5	12-Feb-14	Revise temperature spec and revise PN table for industrial temperature. Revise datasheet format. Revise the tRFC for 4Gb from 300ns to 260ns. Change EEPROM Supply Voltage (min) from 1.7 to 3.0. remove CL10 PN which are not supported at industrial temperature	Bob Desmarais
B	July 20, 2017	Revise logo. Change company address	

STATEMENT OF COMPLIANCE
Viking Technology, Sanmina Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.