A RF, Optical, Microelectronics and Memory Company

US Headquarters
2950 Red Hill Ave, Costa Mesa
California, USA 92626

Office: 714.913.2200
Fax: 714.913.2202

www.vikingtechnology.com

Datasheet for:

SD Card 3.0 / 6.0

PSFSD3xxxxQxxxx

Legal Information

Revision History

Date	Revision	Description	Checked by
1/22/19	E1	Add SD 6.0 PNs: 4GB: VPFSD34096QEWPTL 8GB: VPFSD38192QEDPTL 32GB: VPFSD3032GQCAPTL 64GB: VPFSD3064GQCZPTL Add SPI Bus Mode Protocol	

Ordering Information

Spec	Viking P/N	NAND Process	Density GB	Temperature
SD 6.0	VPFSD34096QEWPTL	TSB 15nm MLC, pSLC	4	-25 to 85°C
SD 6.0	VPFSD38192QEDPTL	TSB 15nm MLC, pSLC	8	-25 to 85°C
SD 6.0	VPFSD3032GQCAPTL	TSB 15nm MLC, pSLC	32	-25 to 85°C
SD 6.0	VPFSD3064GQCZPTL	TSB 15nm MLC, pSLC	64	-25 to 85°C

Table of Contents

1 INTRODUCTION 8

1.1 Features 8

1.2 General Description 10

1.3 Flash Management 10
1.3.1 Error Correction Code (ECC) 10
1.3.2 Wear Leveling 10
1.3.3 Bad Block Management 10
1.3.1 SMART Function 11
1.3.2 Auto-Read Refresh 11
1.3.3 Data Clone System (DCS) 11
1.3.4 Embedded mode 11
1.3.5 Pseudo SLC (pSLC) 12

2 PRODUCT SPECIFICATIONS 13

2.1 Summary 13

2.2 Block Diagram 14

2.3 SD CARD COMPARISON 15

1 ELECTRICAL INTERFACE OUTLINES 16

1.1 SPI Bus Mode Protocol 16

2 ENVIRONMENTAL SPECIFICATIONS 17

2.1 Environmental Conditions 17
2.1.1 Temperature and Humidity 17
2.1.2 Shock and Vibration 17
2.1.1 Electromagnetic Immunity and EMI Compliance 17
2.1.2 Drop 17
2.1.3 Bend 18
2.1.4 Toque 18
2.1.5 Switch 18
2.1.6 Card Socket Insertions 18
2.1.7 Electrostatic Discharge (ESD) 18

2.2 Power Consumption 19

2.3 DC Characteristic 19

2.3.1 Bus Operation Conditions for 3.3V Signaling 19
2.3.2 Bus Signal Line Load 21
2.3.3 Power Up Time of Host 22
2.3.4 Power Up Time of Card 24

2.4 AC Characteristic 25
2.4.1 SD Interface Timing (Default) 25
2.4.2 SD Interface Timing (High-Speed Mode) 28
2.4.3 SD Interface Timing (SDR12, SDR25 and SDR50 Modes) 30
2.4.4 SD Interface Timing (DDR50 Mode) 34

3 INTERFACE 37

3.1 Pad Assignment and Descriptions 37
3.1.1 SD Bus Pin Assignment 37

4 MECHANICAL INFORMATION 39

Table of Tables

Table 2-1: Comparing SD3.0 Standard, SD3.0 SDHC and SD3.0 SDXC 15
Table 2-2: Comparing UHS Speed Grade Symbols 15
Table 3-1: Temperature Specifications 17
Table 3-2: Shock and Vibration Specifications 17
Table 3-3: Drop Specifications 17
Table 3-4: Bend Specifications 18
Table 3-5: Torque Specifications 18
Table 3-6: Switch Specifications 18
Table 3-7: Card Socket Insertions 18
Table 3-8: Electrostatic Discharge (ESD) 18
Table 3-9: Power Consumption 19
Table 3-10: Threshold Level for High Voltage Range 19
Table 3-11: Peak Voltage and Leakage Current 20
Table 3-12: Threshold Level for 1.8V Signaling 20
Table 3-13: Input Leakage Current for 1.8V Signaling 20
Table 3-14: Bus Operation Conditions – Signal Line's Load 21
Table 3-15: Timing Specifications 27
Table 3-16: Card Output Timing (High Speed Card) 29
Table 3-17: Clock Signal Timing 30
Table 3-18: SDR50 and SDR104 Card Input Timing 31
Table 3-19: Output Timing of Fixed Data Window (SDR12, SDR25, SDR50) 32
Table 3-20: Output Timing of Variable Window (SDR104) 33
Table 3-21: Clock Signal Timing 34
Table 3-22: Bus Timings – Parameters Values (DDR50 Mode) 36
Table 4-1: SD Bus Pin Assignment 37
Table 4-2: Registers 38

Table of Figures

Figure 1-1: pSLC 12
Figure 2-1: High-Level Block Diagram 14
Figure 3-1: Bus Circuitry Diagram 21
Figure 3-2: Power Up Time of Host 22
Figure 3-3: Power Up Time of Card 24
Figure 3-4: Voltage Levels 25
Figure 3-5: Card Input Timing (Default Speed Card) 25
Figure 3-6: Card Output Timing (Default Speed Card) 26
Figure 3-7: Card Input Timing (High Speed Card) 28
Figure 3-8: Card Output Timing (High Speed Card) 28
Figure 3-9: Clock Signal Timing (Input) 30
Figure 3-10: SDR50 and SDR104 Card Input Timing 31
Figure 3-11: Clock Signal Timing (Output Timing of Fixed Data) 32
Figure 3-12: Output Timing of Variable Window (SDR104) 33
Figure 3-13: Clock Signal Timing 34
Figure 3-14: Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode 35
Figure 5-1: SD Case Dimensions: 24mm (W) x 32mm (L) x 2.1mm (H) 39
Figure 5-2: SD Dimension Details 40

1 Introduction

Viking SSD's offer the highest flash storage reliability and performance as well as support for many functional features.

1.1 Features

- Flash Type
  - Toshiba 15nm MLC in pSLC mode
- 3.0 Bus Speed Mode
  - UHS-I (4GB and higher)
  - Non-UHS (2GB and lower)
- Speed Class
  - Class 2/6/10
- Power Consumption [Note]
  - Power Up Current < 250uA
  - Standby Current < 1000uA
  - Read Current < 400mA
  - Write Current < 400mA
- CPRM (Content Protection for Recordable Media)
- Advanced Flash Management
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - PPMS
  - SMART function
  - Auto-Read Refresh
  - Embedded Mode
- Write Protect with mechanical switch
- SD SPI Mode
- Supply Voltage 2.7 ~ 3.6V
- Temperature Range
  - Operation: -25°C ~ 85°C
  - Storage: -40°C ~ 85°C
- RoHS compliant
- EMI compliant

NOTE: Please see Chapter on Power Consumption for details

- SD 6.0 Performance Overview

Process	Capacity	Flash Structure	Performance		Power Consumption (Maximum)		
			TestMetrixTest @500MB		Read (mA)	Write (mA)	Standby (mA)
			Read (MB/s)	Write (MB/s)			
pSLC	4GB	8GB x 1	90	80	400	400	1
	8GB	8GB x 2	95	90	400	400	1
	32GB	8GB x 8	95	90	400	400	1
	64GB	16GB x 8	95	90	400	400	1

1.2 General Description

The Secure Digital (SD) card version 3.0 / 6.0 is fully compliant with the standards released by the SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver3.0 / 6.01 Final] definitions. Card capacities of non-secure area and secure area support [Part 3 Security Specification Ver3.0 / 6.0 Final]

The SD 3.0 / 6.0 card has a 9-pin interface, designed to operate at a maximum frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. The Card capacity could be more than 64GB and up to 2TB in the future with ex-FAT file system, which is called SDXC (Extended Capacity SD Memory Card). Secure Digital 3.0 / 6.0 cards are one of the most popular cards today due to its high performance, good reliability and wide compatibility.

1.3 Flash Management

1.3.1 Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, Viking SD cards apply the BCH ECC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption.

1.3.2 Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Viking provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.3.3 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named

“Later Bad Blocks”. Viking implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.3.1 SMART Function

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an special function that allows a memory device to automatically monitor its health. A SmartInfo Tool is used to observe SMART data and will display the controller version, flash type, firmware version, endurance life ratio, good block ratio, and so forth. In addition, a warning message will appear under the following 3 conditions:

(1) When the life ratio remained is less than 10%,

(2) When the amount of abnormal power on is more than 3,500 cycles, and

(3) When there are less than 5 usable blocks for replacing bad blocks.

1.3.2 Auto-Read Refresh

Auto-Read Refresh is especially applied on devices that read data mostly but rarely write data, such as GPS. When blocks are continuously read, then the device cannot activate wear leveling since it can only be applied while writing data. Thus, errors will accumulate and become uncorrectable. Accordingly, to avoid errors exceed the amount ECC can correct and blocks turn bad, Phison’s firmware will automatically refresh the bit errors when the error number in one block approaches the threshold, ex., 24 bits.

1.3.3 Data Clone System (DCS)

DCS is a function which minimizes the chance of data lost in the event of sudden power lost. When power lost occurred during writing, there will always be a chance where the data become corrupted. To counter this, firmware will perform extra writing of data to a buffer block. In the event of a sudden power loss, during the next power up, ECC will be checked on the original target block. If ECC was discovered, the firmware will copy the same data from the buffer block and replace the corrupted data in the original target block. This will greatly reduce the chance of the corrupted data being used continuously.

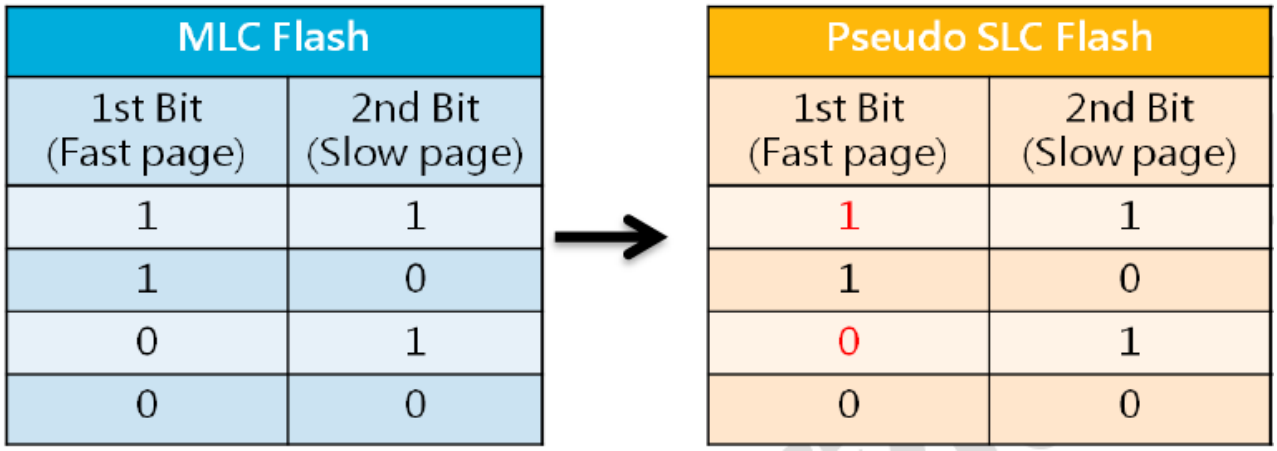
1.3.4 Embedded mode

Embedded mode is a function specially designed for operating systems that do not utilize FAT. Often under non Windows OS, for example Linux or customized host, wear leveling mechanism of SD cards will be affected or even disabled in some cases. With embedded mode activated, SD cards ensure that under any circumstances, wear leveling mechanism can operate normally to keep the usage of blocks even throughout the card’s life cycle. This is especially a great add-on for security cameras or drive recorders.

1.3.5 Pseudo SLC (pSLC)

Pseudo SLC can be considered as an extended version of MLC. While MLC contains fast and slow pages, pSLC only applies fast pages for programming. The concept of pSLC is demonstrated in the two tables below. The first and second bits of a memory cell represent a fast and slow page respectively. Since only fast pages are programmed when applying pSLC, the bits highlighted in red are used, as shown in the right table. Accordingly, because only fast pages are programmed, pSLC provides better performance and endurance than MLC. Moreover, pSLC performs similarly with SLC, yet pSLC is more cost-effective.

Figure 1-1: pSLC



MLC Flash	
1st Bit (Fast page)	2nd Bit (Slow page)
1	1
1	0
0	1
0	0

Pseudo SLC Flash	
1st Bit (Fast page)	2nd Bit (Slow page)
1	1
1	0
0	1
0	0

2 PRODUCT SPECIFICATIONS

2.1 Summary

- Support SD system specification version 3.0 / 6.0
- Card capacity of non-secure area and secure area support
  [Part 3 Security Specification Ver3.0 Final] Specifications

- Support SD SPI mode
- Designed for read-only and read/write cards
- Bus Speed Mode (use 4 parallel data lines)
  - Non-UHS Mode
    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec
    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec
  - UHS Mode
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/sec

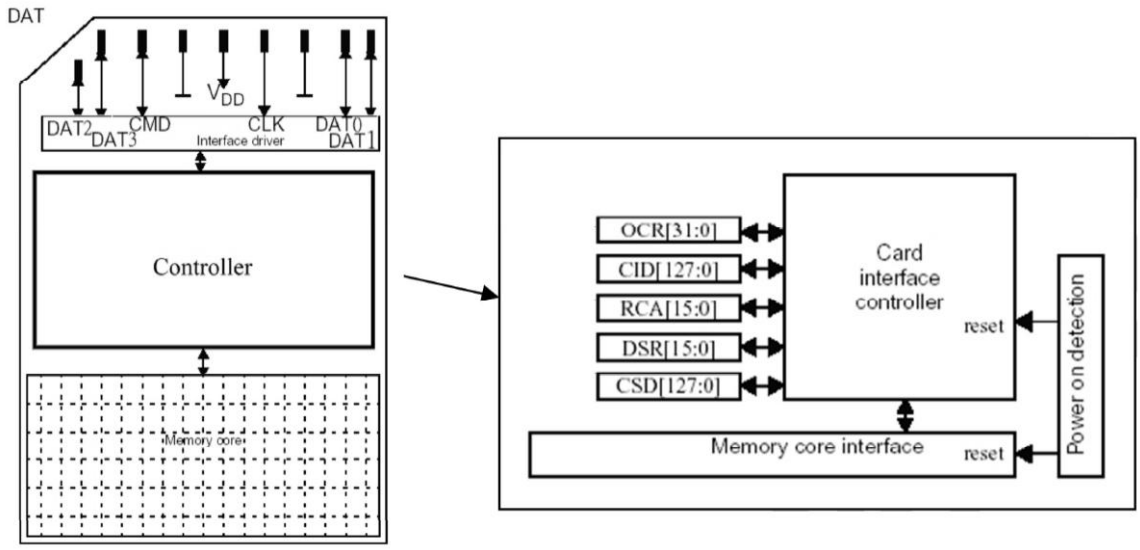
    NOTES:
    1. Timing in 1.8V signaling is different from that of 3.3V signaling.
    2. To properly run the UHS mode, please ensure the device supports UHS-I mode.

- The command list supports
  [Part 1 Physical Layer Specification Ver3.1 Final] definitions

- Copyrights Protection Mechanism
  - Compliant with the highest security of DPRM standard
- Support CPRM (Content Protection for Recordable Media) of SD Card
- Card removal during read operation will never harm the content
- Password Protection of cards (optional)
- Write Protect feature using mechanical switch
- Built-in write protection features (permanent and temporary)
- Electrostatic Discharge (ESD)
  - ESD protection in contact pads (contact discharge)
  - ESD protection in non-contact pads (air discharge)
- Operation voltage range: 2.7 ~ 3.6V
- Support Dynamic and Static Wear Leveling

2.2 Block Diagram

Figure 2-1: High-Level Block Diagram



2.3 SD CARD COMPARISON

Table 2-1: Comparing SD3.0 Standard, SD3.0 SDHC and SD3.0 SDXC

	SD3.0 SDSC (Backward compatible to 2.0 host)	SD3.0 SDHC (Backward compatible to 2.0 host)	SD3.0 SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for operation)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 2-2: Comparing UHS Speed Grade Symbols

	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Operable Under	*UHS-I Bus I/F, UHS-II Bus I/F	
SD Memory Card	SDHC UHS-I and UHS-II, SDXC UHS-I and UHS-II	
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording real-time broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

*UHS (Ultra High Speed), , defines bus-interface speeds up to 312 Megabytes per second for greater device performance. It is available on SDXC and SDHC memory cards and devices.

\

1 ELECTRICAL INTERFACE OUTLINES

1.1 SPI Bus Mode Protocol

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel by byte oriented. Every command or data block is built for 8-bit bytes and is byte aligned with the CS signal (i.e. the length is a multiple of 8 clock cycles). The card starts to count SPI bus clock cycle at the assertion of the CS signal. Every command or data token shall be aligned with 8-clock cycle boundary.

Similar to the SD Memory Card Protocol, the SPI messages consist of command, response and data-block tokens. The advantage of SPI mode is reducing the host design effort, especially for MMC host side, it just be modified by little change. Note: please use SD card specification to implement SPI mode function, not use MMC specification. For example, SPI mode is initialized by ACMD41, and the registers are different from MMC card, especially CSD register.

Refer to SD specification for the state diagram in SPI mode and SPI command set.

2 ENVIRONMENTAL SPECIFICATIONS

2.1 Environmental Conditions

2.1.1 Temperature and Humidity

Table 2-1: Temperature Specifications

Conditions	Operating	Shipping	Storage
Temperature- Ambient	-25 to 85°C	-40 to 85°C	-40 to 85°C
Humidity (non-condensing)	95% under 25C	93% under 40C	93% under 40C

2.1.2 Shock and Vibration

Table 2-2: Shock and Vibration Specifications

Stimulus	Description
Shock	1500G, 0.5ms
Vibration	20 – 80 Hz/1.52mm, 80 – 2000 Hz/20G, (X,Y,Z axis / 30 min for each)

2.1.1 Electromagnetic Immunity and EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

2.1.2 Drop

Table 2-3: Drop Specifications

	Height of Drop	Number of Drop
SD card	150cm free fall	Direction: 6 face; 1 time/face

Result: No any abnormality is detected when power on

2.1.3 Bend

Table 2-4: Bend Specifications

	Force	Action
SD card	≥ 10N	Hold for 1min; total 5 times.

Result: No any abnormality is detected when power on

2.1.4 Toque

Table 2-5: Torque Specifications

	Force	Action
SD card	0.15N-m or ±2.5 deg	Hold 30 second/direction, Total 5 cycles

Result: No any abnormality is detected when power on

2.1.5 Switch

Table 2-6: Switch Specifications

	Force	Number of Switch Cycle
SD card	0.4N-m~5N-m	1000 cycles

Result: No any abnormality is detected when power on

2.1.6 Card Socket Insertions

Table 2-7: Card Socket Insertions

	Number of Mating Cycles	Result
SD card	10000 cycles	Pass

2.1.7 Electrostatic Discharge (ESD)

Table 2-8: Electrostatic Discharge (ESD)

	Condition	Result
SD card	Contact: ±4KV; 5 times/Pin	Pass
	Air: ±15KV; 5 times/Position	Pass

2.2 Power Consumption

The table below is the power consumption of SD card with different bus speed modes.

Table 2-9: Power Consumption

Bus Speed Mode	Max. Power Up Current (uA)	Max. Standby Current (uA)	Max. Read Current (mA)	Max. Write Current (mA)
Default Speed Mode	250	1000	150 @ 3.6V	150 @ 3.6V
High Speed Mode	250	1000	200 @ 3.6V	200 @ 3.6V

NOTES:

1) Power consumptions are measured at room temperature (25C). Standby current might rise to 1600 under 85C.
2) Power consumption of Max. Standby Current is for SD cards under and including 64GB only. For 128GB and 256GB, the power consumption is to be determined.

2.3 DC Characteristic

2.3.1 Bus Operation Conditions for 3.3V Signaling

Table 2-10: Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	VDD	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*VDD		V	I_{OH}=-2mA VDD Min
Output Low Voltage	V_{OL}		0.125*VDD	V	I_{OL}=2mA VDD Min
Input High Voltage	V_{IH}	0.625*VDD	VDD+0.3	V	
Input Low Voltage	V_{IL}	VSS-0.3	0.25*VDD	V	
Power Up Time			250	ms	From 0V to VDD min

Table 2-11: Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 2-12: Threshold Level for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.58	V	

Table 2-13: Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected

2.3.2 Bus Signal Line Load

Figure 2-1: Bus Circuitry Diagram

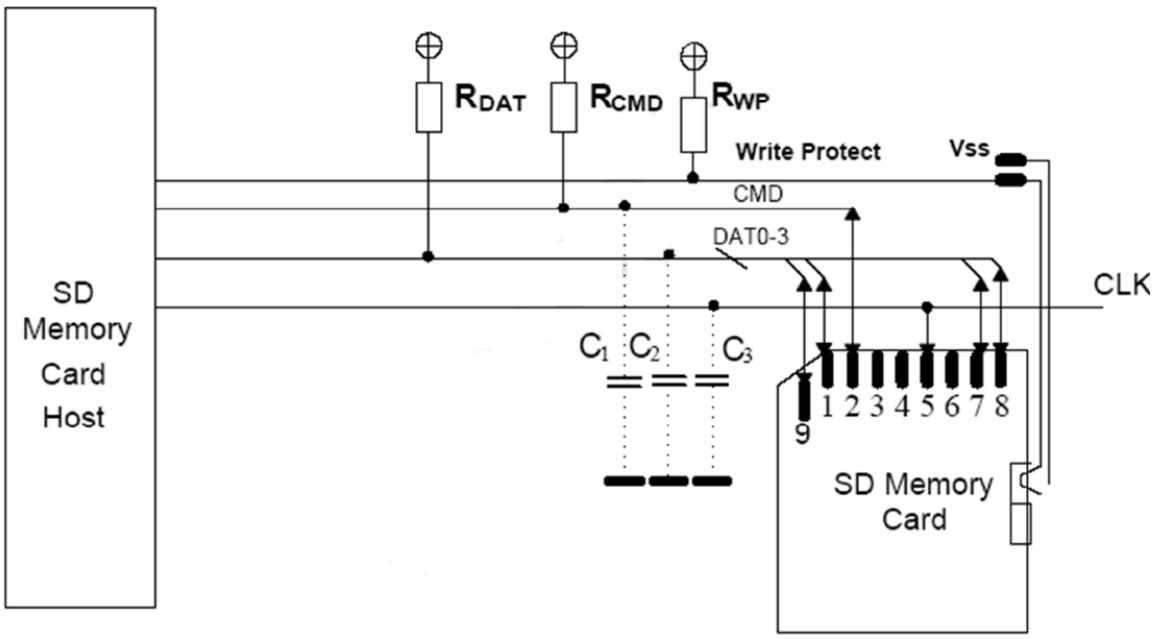


Table 2-14: Bus Operation Conditions – Signal Line's Load

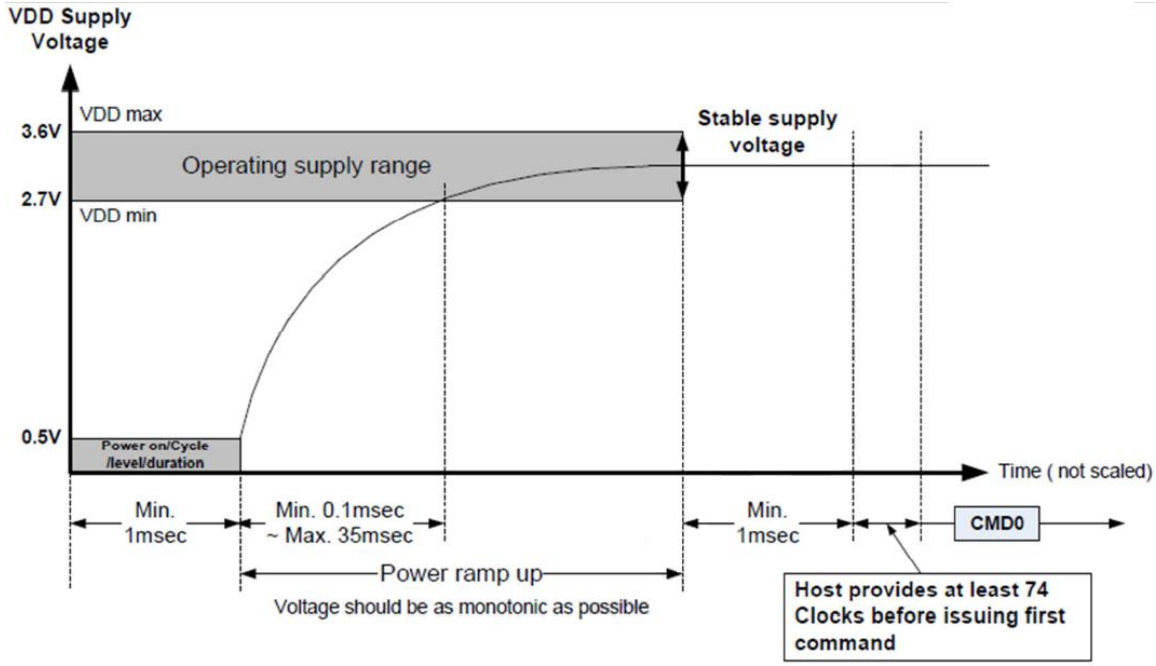
Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	To prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

Notes:
Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

2.3.3 Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

Figure 2-2: Power Up Time of Host



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

1. Voltage level shall be below 0.5V
2. Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendations of Power ramp up:

1. Voltage of power ramp up should be monotonic as much as possible.
2. The minimum ramp up time should be 0.1ms.
3. The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
4. Host shall wait until VDD is stable.
5. After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

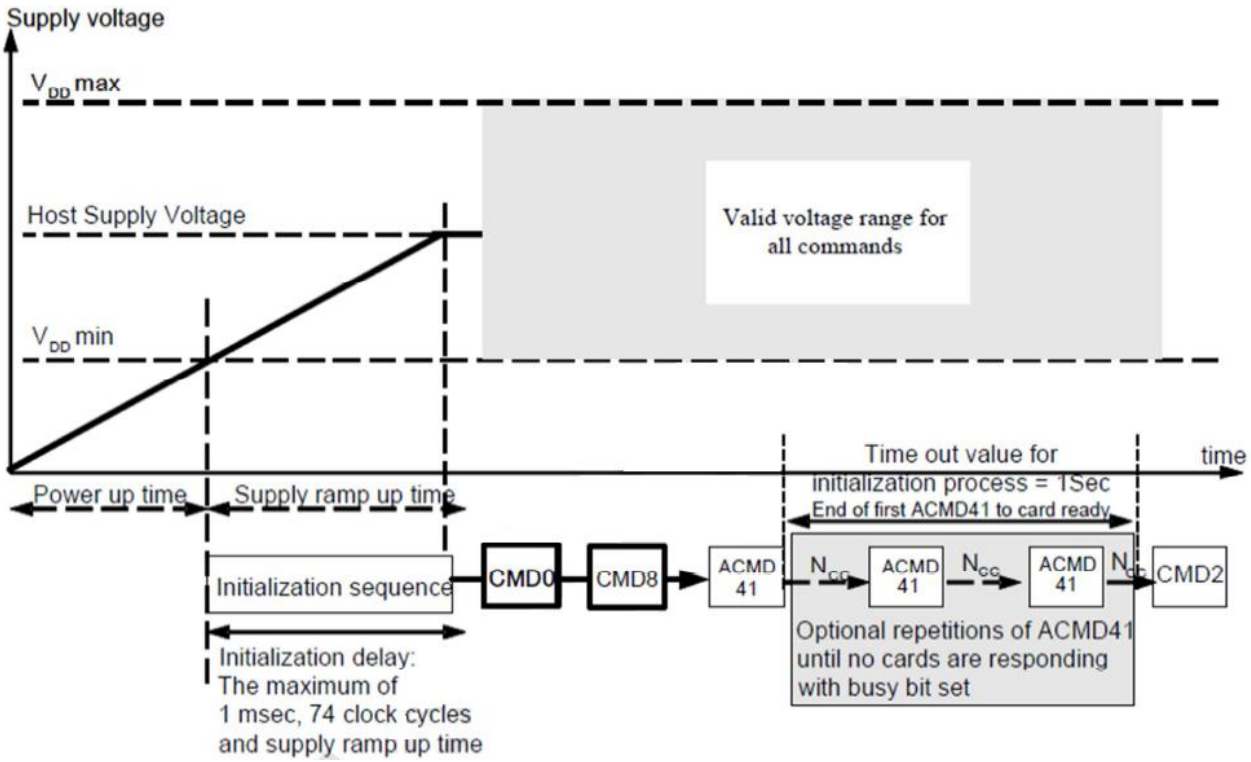
Power Down and Power Cycle

1. When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
2. If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

2.3.4 Power Up Time of Card

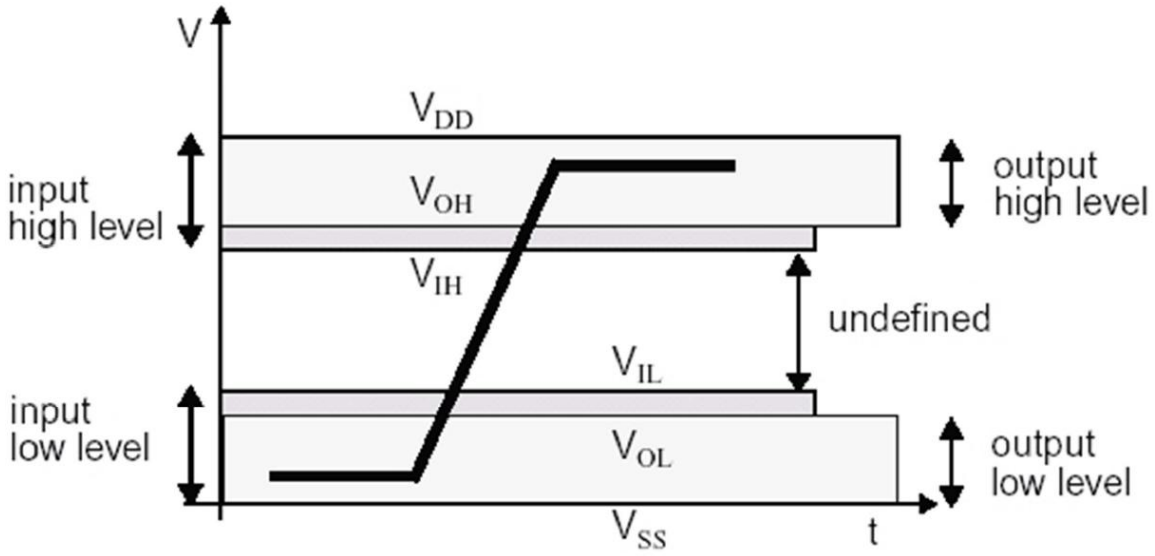
A device shall be ready to accept the first command within 1ms from detecting VDD min. Device may use up to 74 clocks for preparation before receiving the first command.

Figure 2-3: Power Up Time of Card



2.4 AC Characteristic

Figure 2-4: Voltage Levels



2.4.1 SD Interface Timing (Default)

Figure 2-5: Card Input Timing (Default Speed Card)

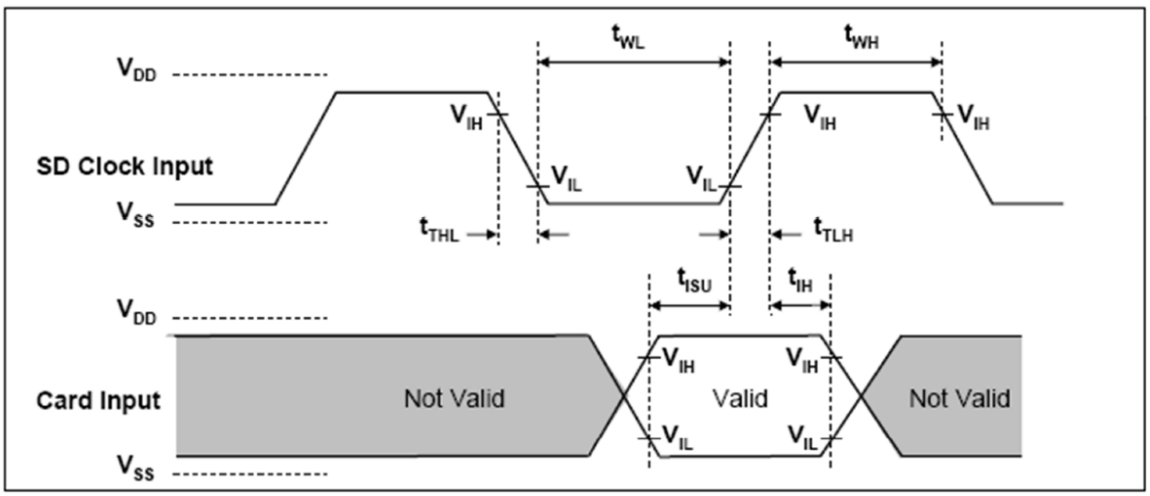


Figure 2-6: Card Output Timing (Default Speed Card)

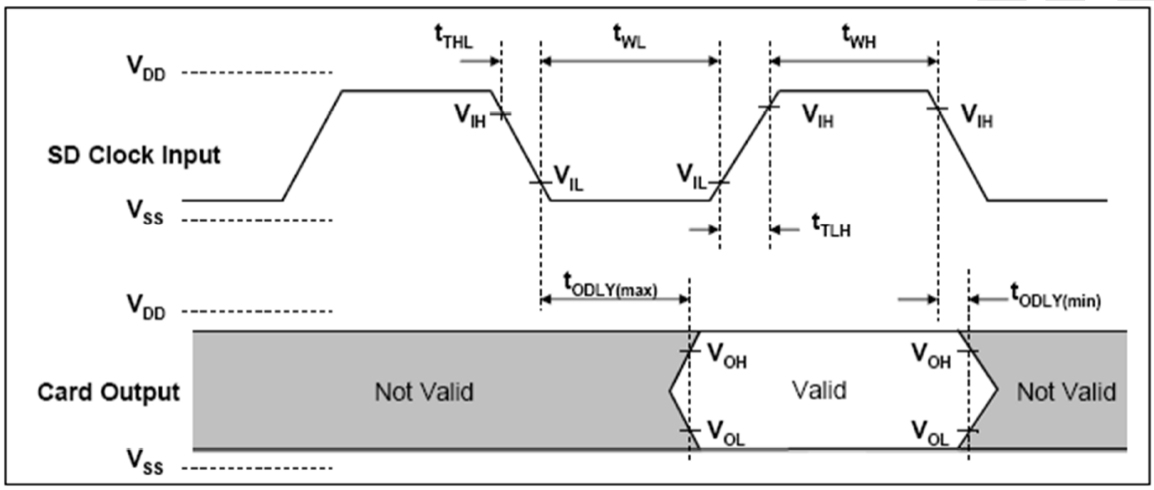


Table 2-15: Timing Specifications

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(VIH) and max(VIL)					
Clock frequency Data Transfer Mode	fPP	0	25	MHz	C_{card}≤10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	C_{card}≤10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_{card}≤40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_{card}≤40 pF (1 card)

Notes:

1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

2.4.2 SD Interface Timing (High-Speed Mode)

Figure 2-7: Card Input Timing (High Speed Card)

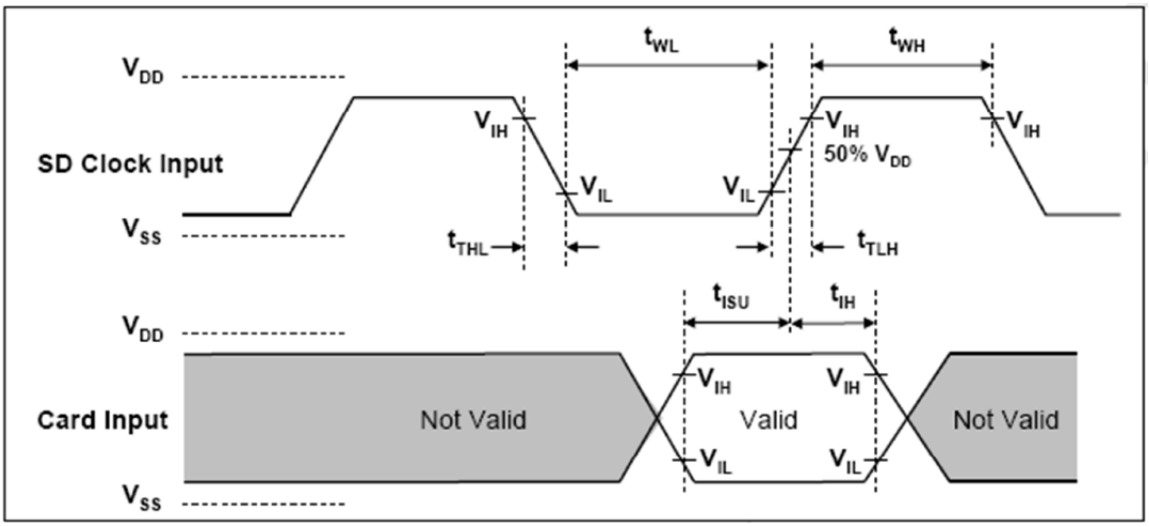


Figure 2-8: Card Output Timing (High Speed Card)

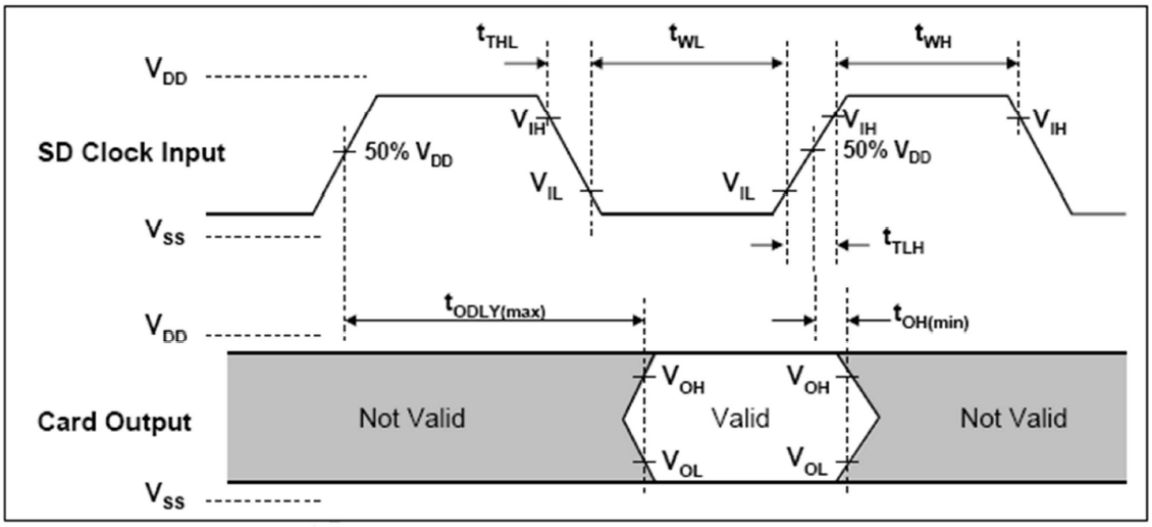


Table 2-16: Card Output Timing (High Speed Card)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(VIH) and max(VIL)					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card}≤10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card}≤10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card}≤10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card}≤10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card}≤10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card}≤10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_{card}≤40 pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_{card}≤15 pF (1 card)
Total System capacitance of each	C_L	0	40	ns	C_{card}≤15 pF (1 card)

Notes:
1) In order to satisfy severe timing, the host shall drive only one card.

2.4.3 SD Interface Timing (SDR12, SDR25 and SDR50 Modes)

Figure 2-9: Clock Signal Timing (Input)

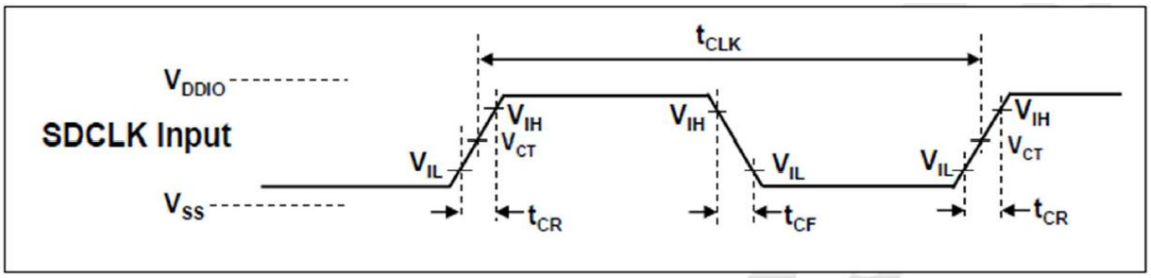


Table 2-17: Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
				t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Figure 2-10: SDR50 and SDR104 Card Input Timing

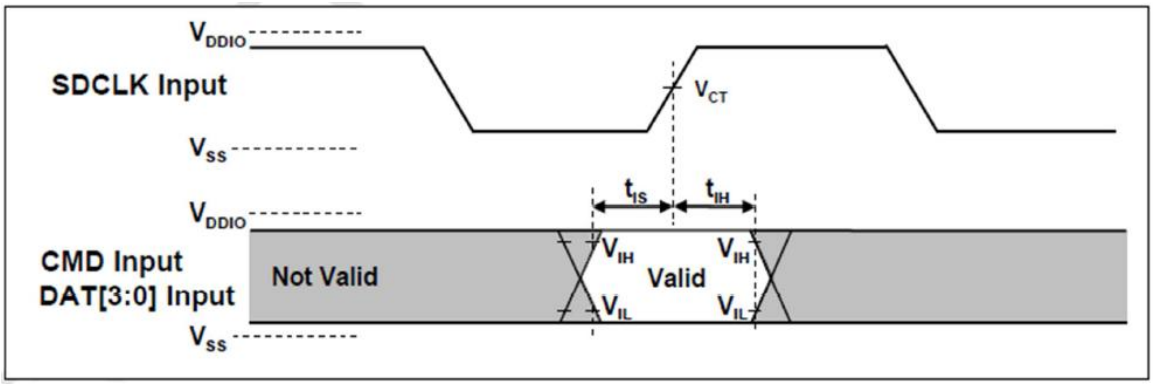


Table 2-18: SDR50 and SDR104 Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.4	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8 1	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V
Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8[1]	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V

Figure 2-11: Clock Signal Timing (Output Timing of Fixed Data)

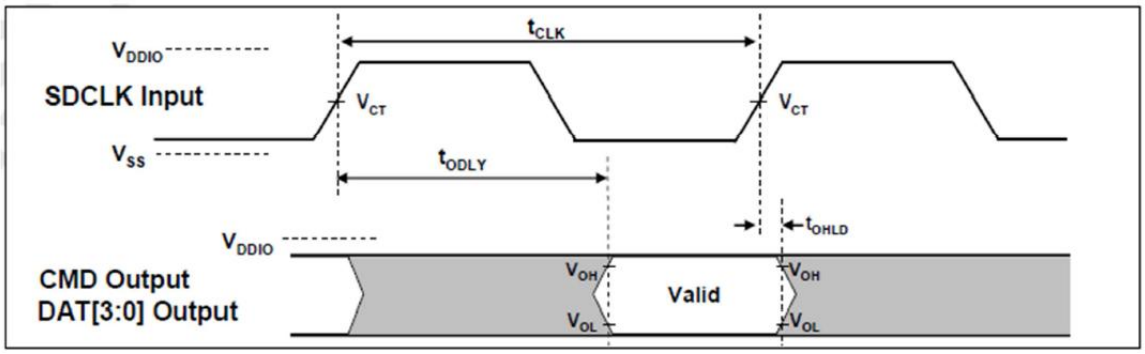


Table 2-19: Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Figure 2-12: Output Timing of Variable Window (SDR104)

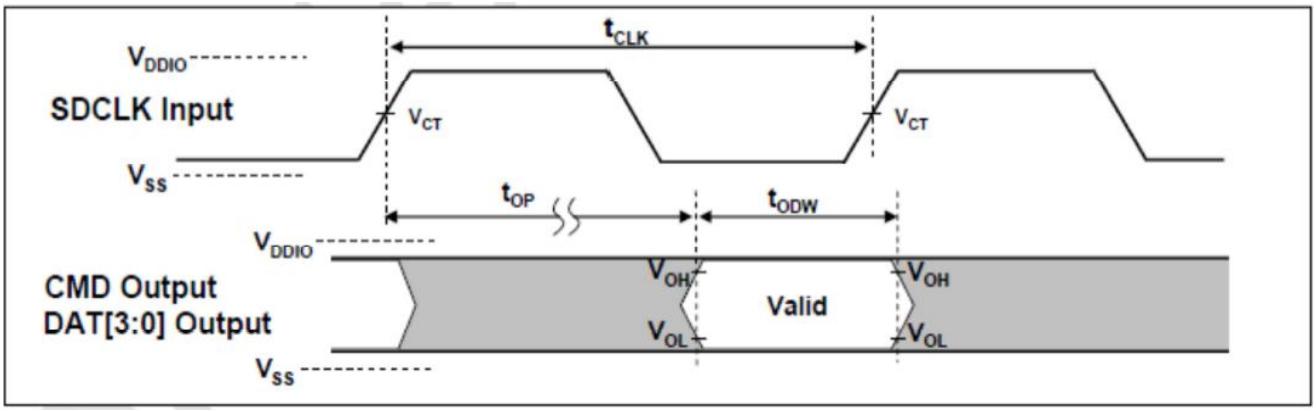


Table 2-20: Output Timing of Variable Window (SDR104)

Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.6	-	UI	t_{ODW} = 2.88ns at 208MHz

2.4.4 SD Interface Timing (DDR50 Mode)

Figure 2-13: Clock Signal Timing

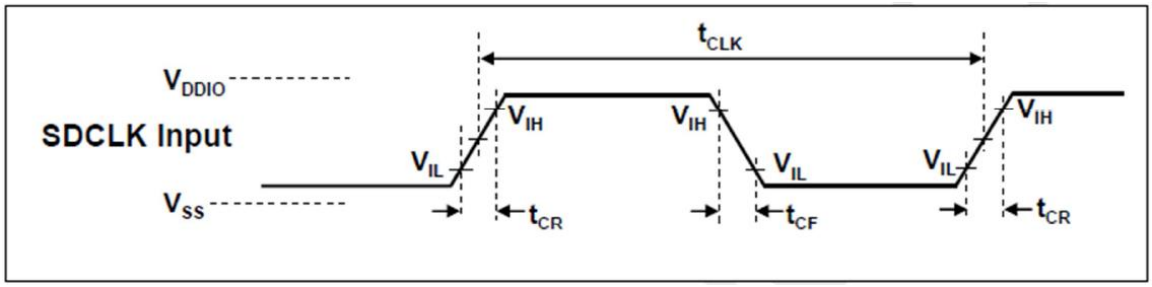


Table 2-21: Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

Figure 2-14: Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

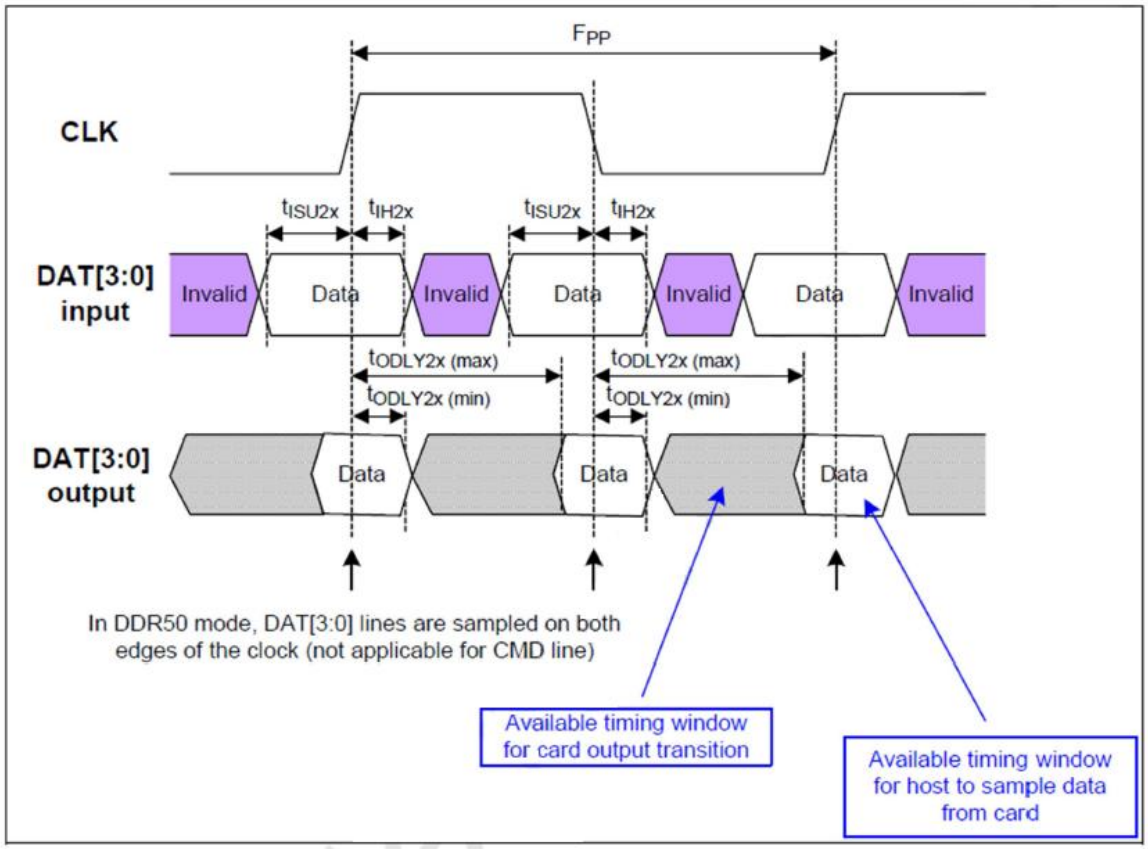


Table 2-22: Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Inputs CMD (referenced to CLK)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤10 pF (1 card)
Outputs CMD (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	13.7	ns	C_L≤30 pF (1 card)
Output hold time	t_{OH}	1.5		ns	C_L≥15 pF (1 card)
Inputs DAT(referenced to CLK)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤10 pF (1 card)
Outputs DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	0	13.7	ns	C_L≤25 pF (1 card)
Output hold time	t_{OH2x}	1.5		ns	C_L≥15 pF (1 card)

3 INTERFACE

3.1 Pad Assignment and Descriptions

3.1.1 SD Bus Pin Assignment

Table 3-1: SD Bus Pin Assignment

Pin #	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	I/O/PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	V_{SS2}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2	I/O/PP	Data Line [Bit 2]	RSV		

Notes:

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

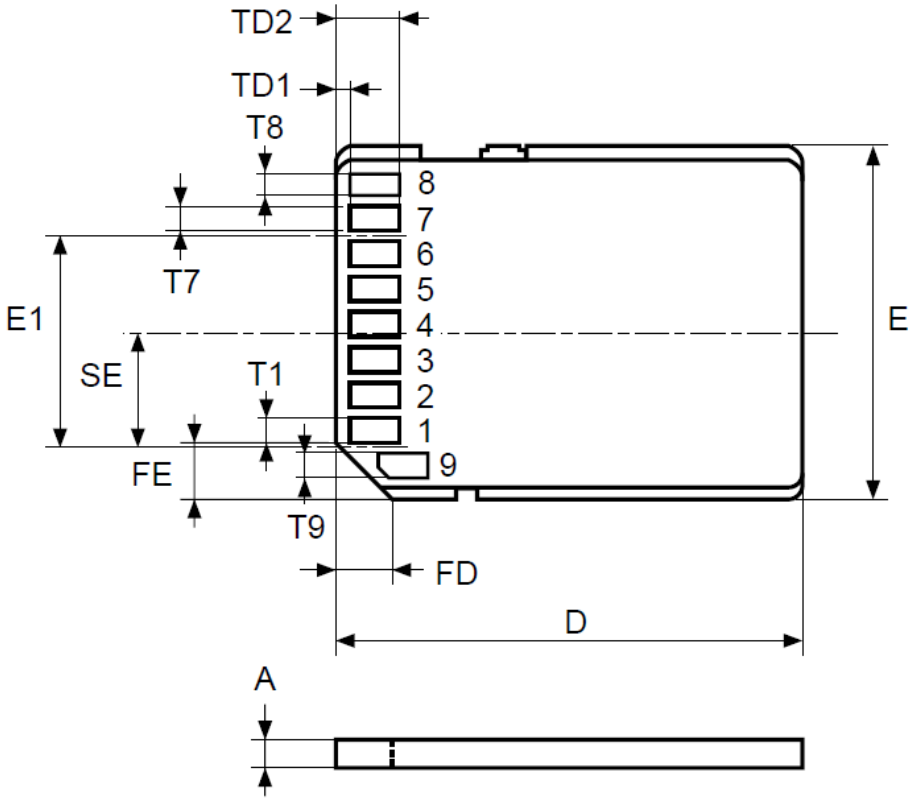
Table 3-2: Registers

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities. **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory**
SSR	512bit	SD Status; information about the card proprietary features. **Mandatory**
OCR	32bit	Card Status; information about the card status. **Mandatory**

Notes:
1) RCA register is not used (available) in SPI mode

4 Mechanical Information

Figure 4-1: SD Case Dimensions: 24mm (W) x 32mm (L) x 2.1mm (H)



Note: Drawing is not to scale

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	2.100	2.050	2.250	0.0827	0.0807	0.0886
D	32.000	31.900	32.100	1.2598	1.2559	1.2638
E	24.000	23.900	24.100	0.9449	0.9409	0.9488
E1	15.000	–	–	0.5906	–	–
FD	4.000	3.900	4.100	0.1575	0.1535	0.1614
FE	4.000	3.900	4.100	0.1575	0.1535	0.1614
SE	8.125	–	–	0.3198	–	–
T1	–	1.400	–	–	0.0551	–
T9	–	1.400	–	–	0.0551	–
T8	–	0.900	–	–	0.0353	–
T7	–	1.100	–	–	0.04331	–
TD1	–	–	1.600	–	–	0.06299
TD2	–	5.000	–	–	0.19685	–

Figure 4-2: SD Dimension Details